PCI Express
SFF-8639 Module

Specification

Revision 3.0, Version 0.9

February 22, 2018

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Revision History

Revision	Version	History	Date
3.0		Initial draft 0.3	June 26, 2013
3.0		Initial draft 0.5	September 10, 2013
3.0	0.3	Updated the following Figures: • Figure 1-1. Vertical SFF-8639 Receptacle • Figure 1-2 • Figure 2-3 through Figure 2-9 • Figure 4-1 through Figure 4-5. Jitter Budget • Figure 5-1. Illustration of Adjacent Pairs • Added Table 2-3 • Global changes: - Replaced REFCLK with REFCLK(B) - Replaced PERST# with PERST(B)#.	August 6, 2014
3.0	0.4	Due to the very large number of changes to the revision 0.9 specification the revision level was reverted to 0.7. • Global changes: - Replaced REFCLK(B) with REFCLK - Replaced PERST# with PERST#. • Updated Figure 2-1, Figure 2-10, Figure 2-11, and Figure 2-13 • Replaced REFCLK(B)- to REFCLK- • Replaced PERSTB(B)# with PERSTB# • Replaced IFDET with IfDet • Replaced +3.3 Vaux with +3.3 Vaux • General clean-up	September 6, 2016
3.0	0.5	• Added PWRDIS (Optional) to Auxiliary Signals • Added PWRDIS Electrical Characteristics • Added Table 2-6, PWRDIS DC and AC Electrical Characteristics Applied to the SFF-8639 Module • Miscellaneous fixes • Incorporated the MAY Integrated 0p705 Draft SFF Connector Comment List Round 11 • Incorporated the Integrated0p706 Draft SFF Connector Comment List Round12 • Incorporated the Integrated0p706 June30 DraftSFF Connector Comment List Round14	July 20, 2017
3.0	0.6	• Added reference to +12 V power to section 2.8, PWRDIS (Optional) • Updated Table 2 4 and Table 2 6. • Incorporated Oct 04 Comments, Round 16 • Incorporated Oct 04 Comments, Round 17 • Incorporated Nov 07 Comments, Round 18	December 19, 2017
3.0	0.9	• Fixed typo in Table A-1. • Rolled Revision to .09	February 27, 2018

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171 # 1. SFF-8639 Connector Interface

172 The focus of this specification is on PCI Express® (PCIe) solutions utilizing the SFF-8639
173 connector interface. Form factors include, but are not limited to, those described in the *SFF-8201*
174 *Form Factor Drive Dimensions Specification*. Other form factors, such as PCI Express® CEM are
175 documented in other independent specifications.

176 ## 1.1. Document Organization

177 The *PCI Express SFF-8639 Module Specification* is a companion specification to the *PCI Express Base*
178 *Specification*.

179 ## 1.2. Capitalizations

180 Some terms in this specification are capitalized to distinguish their definition in the context of this
181 document from their common English meaning. Words not capitalized have their common English
182 meaning. When terms such as *memory write* or *memory read* appear completely in lower case, they
183 include all transactions of that type.

184 ## 1.3. Terms and Definitions

185 Following are terms and acronyms used in this specification. Terms and Acronyms not defined in
186 this section are found in the *PCI Express Base Specification* or the *PCI Express CEM Specification.*

Dual port mode	When enabled, lanes 0 and 1 form a x2 port (A-side) and lanes 2 and 3 form a second x2 port (B-side). The A and B side PCI Express interfaces must operate independently with any combination of active / inactive states possible. Any other interaction between the A and B side interfaces is outside the scope of this specification. When the Dual port mode is disabled, all four lanes form a single x4 port.
Hot-Plug	Insertion and/or removal of an SFF-8639 module into an active backplane or system board as defined in *PCI Standard Hot-Plug Controller and Subsystem Specification*.

Receiver path	The path from the SFF-8639 receptacle to the Receiver for a differential data pair (system) or the SFF-8639 plug to the Receiver (SFF-8639 module).
Reference Receiver	A Receiver model consisting of behavioral CTLE, DFE and Receiver load models.
SFF-8639 bay	The system side of the SFF-8639 module to system interface.
SFF-8639 module	A module that includes the SFF-8639 plug.
SFF-8639 plug	The free side of the SFF-8639 connector interface.
SFF-8639 receptacle	The fixed side of the SFF-8639 connector interface.
SFF-8639 system-side	Includes the system board (or Switch Add-in Card if applicable), SFF-8639 receptacle and all interconnect between those two points. The SFF-8639 module is not included.
Transmitter path	The path from the Transmitter to the SFF-8639 receptacle for a differential data pair (system) or the Transmitter to the SFF-8639 plug (SFF-8639 module).
wakeup	A mechanism used by a component to request the reapplication of main power when in the L2 Link state. Two such mechanisms are defined in the *PCI Express Base Specification*: Beacon and WAKE#. This specification requires the use of WAKE# on any SFF-8639 module or system that supports wakeup functionality.

1.4. Reference Documents

This specification references the following documents:

- *PCI Express Base Specification,* Revision 3.0
- *PCI Local Bus Specification,* Revision 3.0
- *PCI Express Jitter Modeling,* Revision 1.0
- *PCI Express Jitter and BER,* Revision 1.0
- *SFF-8201: 2.5" Form Factor Drive Dimensions,* Revision 3.3
- *SFF-8223: 2.5" Form Factor Drive with Serial Attached Connector,* Revision 2.7
- *SFF-8639: Multifunction 6X Unshielded Connector,* Revision 2.0
- *SFF-9639: Multifunction 6X Unshielded Connector Pinouts,* Revision 1.0
- *System Management Bus (SMBus) Specification,* Version 2.0
- *PCI Standard Hot-Plug Controller and Subsystem Specification,* Revision 1.0
- *PCI Hot-Plug Specification,* Revision 1.1
- *PCI Bus Power Management Interface Specification*, Revision 1.2
- *PCI Express Architecture, PHY Test Specification,* Revision 3.0

1.5. Specification Contents

This specification contains the following information:

- Auxiliary signals
- Hot insertion and removal
- Power delivery
- Electrical budget
- Connector specification
- Form factors and implementation
- System requirements

1.6. Objectives

The objectives of this specification are:

- Support 8.0 GT/s data rate (per direction)
- Support 5.0 GT/s data rate (per direction)
- Support 2.5 GT/s data rate (per direction)
- Enable Hot-Plug and Hot swap
- Leverage storage industry commonality
- Facilitate smooth transitions
- Allow co-existence of both SFF-8639 modules and existing storage products
- Extensible for future bandwidth needs
- Maximize SFF-8639 module interoperability for user flexibility
- Upgradeability
- Enhanced end user experience

1.7. Electrical Overview

The electrical specification covers Auxiliary signals, hot insertion and removal, power delivery, and interconnect electrical budgets. The PCI Express Transmitter and Receiver electrical requirements are specified in the *PCI Express Base Specification*.

In addition to those signals required to transmit/receive data on the PCI Express interface, there are other signals that are available to implement the PCI Express interface in a system environment, or to provide certain desired functions. These signals are referred to as the Auxiliary signals. They include:

- Reference clock (REFCLK+/REFCLK-): this signal must be supplied by the system (see Section 2.1.1).
- PRSNT#, IfDet#: SFF-8639 module presence detect pins (required).
- PERST#: PCI Express reset, required.
- ACTIVITY#: Indicates activity of the SFF-8639 module, required.
- SMBus (SMBCLK and SMBDAT), *System Management Bus (SMBus) Specification*, optional.
- Wake (WAKE#): This signal is required only if the module/system supports wakeup and/or the Optimized Buffer Flush/Fill (OBFF) mechanism.
- +3.3 Vaux: Auxiliary power, supports SMBus and wakeup functionality, optional.
- DualPortEn#: This signal is asserted to enable Dual port mode of the SFF-8639 module and de-assert to default to a single x4 port, optional.
- REFCLKB+ and REFCLKB-: These reference clock signals - must be provided by the system to the module if Dual port mode is enabled and the B-side port system is enabled.
- PERSTB#: This signal is required if Dual port mode is enabled by the system and supported by the module.
- CLKREQ#: This signal is required if the module needs to control the clock or if L1 PM Substates are supported; not supported if Dual port mode enabled.
- PWRDIS: This signal is asserted to disable power to the SFF-8639 module circuitry.

The signals REFCLK+, REFCLK-, REFCLKB+, REFCLKB-, SMBCLK, SMBDAT, PERST#, PERSTB#, ACTIVITY#, DualPortEn#, CLKREQ#, PWRDIS, and WAKE# are described in Chapter 2, *Auxiliary Signals*. The signals PRSNT# and IfDet# are described in Chapter 3, *Hot Insertion and Removal*. The signal +3.3 Vaux is described in Chapter 4, *Electrical Requirements*.

Chapter 3, *Hot Insertion and Removal*; discusses the detailed implementation of PCI Express Hot-Plug.

Chapter 4, *Electrical Requirements,* specifies the SFF-8639 module electrical requirements, which include power delivery and interconnect electrical budgets. Power is delivered from the system to the module via the SFF-8639 connector, using two voltage rails:
+3.3 Vaux and +12 V. A +5 V power rail may be present on the SFF-8639 receptacle, but all details are outside the scope of this specification. . Note that the +3.3 Vaux voltage rail is not required for all platforms (see Section 4.1 for more information on the required usage of +3.3 Vaux). Chapter 4, *Electrical Requirements* also describes interconnect electrical budgets; focusing on the system and SFF-8639 module loss and jitter requirements.

1.8. Mechanical Overview

An example of the vertical SFF-8639 receptacle is shown in Figure 1-1.

Note: Right-angle receptacles are also expected to be available.

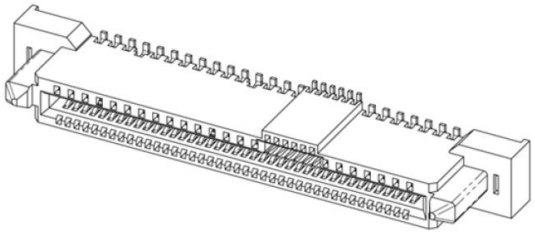

Figure 1-1. Vertical SFF-8639 Receptacle

The SFF-8639 module with a backplane as the interface to the system is shown in Figure 1-2.

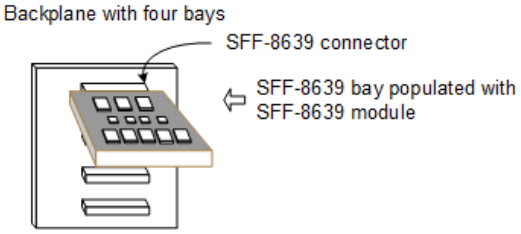

Figure 1-2. Backplane Application

While the reality of multiple variations of SFF-8639-connected architectures is recognized, no attempt will be made to define every possible variation in this specification. This specification, instead, focuses on the vertical SFF-8639 receptacle and form factor requirements by covering the following:

- Specifications for the SFF-8639 connector mating interfaces, footprints and form factors
- Electrical, mechanical, and reliability requirements of the connectors, including the connector testing procedures

Connector definitions and requirements are addressed in Chapter 5, *SFF-8639 Connector Specification* and SFF-8639 form factors and implementation details are discussed in Chapter 6, *SFF-8639 Module Form Factor*.

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286 # 2. Auxiliary Signals

287 The Auxiliary signals are provided on the SFF-8639 module connector interface to assist with
288 certain system-level functionality or implementation. The SFF-8639 module connector interface
289 supports the following Auxiliary signals:

290 - REFCLK+/REFCLK-: These are low voltage differential signals. A system board that supports
291 5.0 GT/s maximum rate signaling or 8.0 GT/s maximum rate signaling must provide a reference
292 clock that meets all requirements[1] for the common clock architecture defined for the reference
293 clock in the *PCI Express Base Specification* and all the requirements defined in this specification. A
294 system board that only supports 2.5 GT/s signaling must meet all reference clock requirements in
295 this specification. The SFF-8639 system must comply with the system board reference clock
296 requirements specified in the *PCI Express Base Specification* and this specification.

297

Note: Reference Clock requirements for 2.5 GT/s, 5.0 GT/s, and 8.0 GT/s signaling rates are defined in this specification. Additional Reference Clock requirements for 5.0 GT/s and 8.0 GT/s signaling rates are defined in the *PCI Express Base Specification*.

298

299 - PERST#: This signal indicates when the applied main power is within the specified tolerance
300 and stable. PERST# goes inactive after a delay of T_{PVPERL} time from the power rails achieving
301 specified tolerance on power up. PERST# is also asserted to reset the SFF-8639 module.
302 - WAKE#: This signal is an open-drain, active low signal that is driven low by a PCI Express
303 Function to re-activate the PCI Express Link Hierarchy's main power rails and reference clocks.
304 It is required on any SFF-8639 module or system board that supports wakeup functionality
305 compliant with this specification. WAKE# is also used by the system to signal to the PCI
306 Express Function in conjunction with the OBFF mechanism.
307 - SMBCLK (optional): This is the SMBus interface clock signal. It is an open-drain signal.
308 - SMBDAT (optional): This is the SMBus interface address/data signal. It is an open-drain signal.
309 - PRSNT#: This signal is the SFF-8639 module presence detect pin. See Chapter 3 for a detailed
310 description.

[1] The RMS jitter requirements are excluded. They are covered under the two-port motherboard test methodology and requirements defined in this specification.

- IfDet#: This signal is the SFF-8639 module interface detect pin. See Chapter 3 for a detailed description.
- ACTIVITY#: This signal indicates activity of the SFF-8639 module.~~Usage of the Activity signal is outside the scope of this specification~~.
- DualPortEn# (optional): This signal is an open drain pulled high by the SFF-8639 module and asserted low by the system to enable Dual port mode of the SFF-8639 module.
- REFCLKB+/REFCLKB- (optional): These are low voltage differential signals. Reference clock for the B-side port interface of the SFF-8639 module. Required from the system if Dual port mode is supported and DualPortEn# is asserted. All other REFCLK+/REFCLK- requirements within this document must apply to REFCLKB+/REFCLKB- unless otherwise noted. Timing requirements for REFCLK+/REFCLK- must apply to REFCLKB+/REFCLKB- with respect to the applicable B-side port signals.
- PERSTB# (optional): This signal is reset for the B-side port interface of the SFF-8639 module. Required from the system if Dual port mode is supported and DualPortEn# is asserted. All other PERST# requirements within this document must apply to PERSTB# unless otherwise noted. Timing requirements for PERST# must apply to PERSTB# with respect to the applicable
  B-side port signals.
- CLKREQ# (optional): This is an open drain signal that enable the PCI Express Clock for the SFF-8639 module and control entry into the L1 PM Substates. CLKREQ# is only valid when the module is not in Dual port mode.
- PWRDIS (optional): This signal is used to disable power to the SFF-8639 module circuitry.

Note that the SMBus interface pins are optional for both the SFF-8639 module and the SFF-8639 system. If the optional management features are implemented, SMBCLK and SMBDAT are both required.

2.1. Reference Clock

2.1.1. Low Voltage Swing, Differential Clocks

Differential clocks are used to reduce jitter and allow for future silicon fabrication process changes and low voltage swing, as shown in Figure 2-1. The nominal single-ended swing for each clock is 0 V to 0.7 V and a nominal frequency of 100 MHz with a tolerance of ±300 ppm. The clock has a defined crossover voltage range and monotonic edges through the input threshold regions as specified in Chapter 4.

Note: If Dual port mode enabled, reference clock requirements apply to the applicable B-side port signals (REFCLKB+ / REFCLKB-). All reference clock requirements apply independently to both ports.

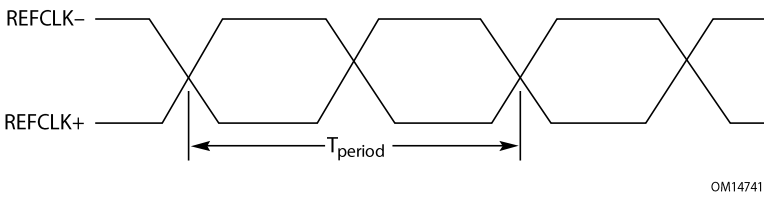


Figure 2-1. Differential REFCLK Waveform

The reference clock pair is routed point-to-point to each SFF-8639 module from the system board to best-known clock routing rules. The transport delay delta between the data and clock at the Receiver is assumed to be less than 12 ns. The combination of the maximum reference clock mismatch and the maximum channel length will contribute approximately 9 ns to 10 ns and the remaining time is allocated to the difference in the insertion delays of the Transmitter and Receiver devices. The routing of each signal in any given clock pair between the clock source and the SFF-8639 module connector interface must be well matched in length (< 0.005 inch) and appropriately spaced away from other non-clock signals to avoid excessive crosstalk.

The SFF-8639 module is required to maintain the 600 ppm data rate matching specified in the *PCI Express Base Specification*.

The system board must provide any termination circuitry required for the reference clock. An example termination topology for a current-mode clock generator is shown in Figure 2-2. EMI emissions will be reduced if clocks to open sockets are shut down at the clock source.

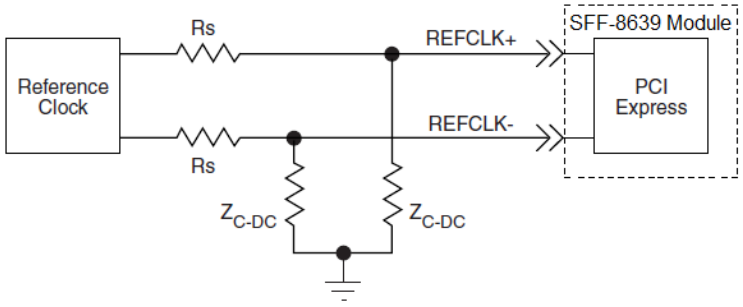


Figure 2-2. Example Current Mode Reference Clock Source Termination

Termination on the SFF-8639 module is allowed, but is not covered by this specification. The same measurement techniques are used as specified in Section 2.1.3. Receiver termination will reduce the nominal swing and rise and fall times by half. The low input swing and low slew rates need to be validated against the clock Receiver requirements as they cause excessive jitter in some clock input buffer designs.

The reference clock timings are based on nominal 100 Ω, differential pair routing with approximately 0.127 mm (5 mil) trace widths. This timing budget allows for a maximum SFF-8639 module trace length of 4.0 inch. No specific trace geometry, however, is explicitly defined in this specification.

2.1.2. Spread Spectrum Clocking (SSC)

Reference clock support of spread spectrum clocking is optional for any given system design due to platform-level timing issues. The minimum clock period must not be violated. The required method is to adjust the spread technique to not allow for modulation above the nominal frequency. This technique is often called *down-spreading*. The requirements for spread spectrum modulation rate and magnitude are given in the *PCI Express Base Specification*.

2.1.3. REFCLK AC Specifications

All specifications in Table 2-1 are to be measured using a test configuration as described in Note 11 with a circuit, as shown in Figure 2-9. All other figure references are given in the Notes section of the table.

382 **Table 2-1. REFCLK DC Specifications and AC Timing Requirements**

Symbol	Parameter	100 MHz Input		Units	Notes
		Min	Max		
Rising Edge Rate	Rising Edge Rate.	0.6	4.0	V/ns	2, 3
Falling Edge Rate	Falling Edge Rate.	0.6	4.0	V/ns	2, 3
V_{IH}	Differential Input High Voltage.	150		mV	2
V_{IL}	Differential Input Low Voltage.		-150	mV	2
V_{CROSS}	Absolute crossing point Voltage.	250	550	mV	1, 4, 5
$V_{CROSS\ DELTA}$	Variation of VCROSS over all rising clock edges.		140	mV	1, 4, 9
V_{RB}	Ring-back Voltage Margin.	-100	100	mV	2, 12
T_{STABLE}	Time before VRB is allowed.	500		ps	2, 12
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy.	-300	2800	ppm	2, 10, 13
$T_{PERIOD\ ABS}$	Absolute Period (including Jitter and Spread Spectrum modulation).	9.847	10.203	ns	2, 6
$T_{CCJITTER}$	Cycle to Cycle Jitter.		150	ps	2
V_{MAX}	Absolute Max input Voltage.		+1.15	V	1, 7
V_{MIN}	Absolute Min input Voltage.		- 0.3	V	1, 8
Duty Cycle	Duty Cycle	40	60	%	2
Rise-Fall Matching	Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching.		20	%	1, 14
Z_{C-DC}	Clock source DC impedance.	40	60	Ω	1, 11

Notes:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 2-7.
4. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 2-3 and Figure 2-4.
5. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 2-3.
6. Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation. See Figure 2-6.
7. Defined as the maximum instantaneous voltage including overshoot. See Figure 2-3.
8. Defined as the minimum instantaneous voltage including undershoot. See Figure 2-3.
9. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in V_{CROSS} for any system. See Figure 2-4.
10. Refer to the *PCI Express Base Specification* for information regarding ppm considerations.
11. System board compliance measurements must use the test load card described in Figure 2-9. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe are used for differential measurements. Test load CL = 2 pF.
12. T_{STABLE} is the time the differential clock must maintain a minimum ±150 mV differential voltage after rising/falling edges before it is allowed to droop back into the V_{RB} (±100 mV) differential range. See Figure 2-8.
13. The acronym ppm refers to *parts per million* and is a DC absolute period accuracy specification. For example, 1 ppm is 1/1,000,000th of 100 MHz exactly or 100 Hz. For 300 ppm, then we have an error budget of 100 Hz/ppm * 300 ppm = 30 kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater. The ±300 ppm applies to systems that do not employ Spread Spectrum Clocking, or that use common clock source. For systems employing Spread Spectrum Clocking there is an additional 2500 ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2800 ppm.
14. To obtain the Rise-Fall Matching parameter, the rising edge rate of REFCLK+ and the falling edge rate of REFCLK- are measured using a ±75 mV window centered on the median crossing point where a rising REFCLK+ crosses a falling REFCLK-. The percentage difference is then calculated by subtracting the slower edge rate from the faster edge rate and dividing the result by the slower edge rate. See Figure 2-5.

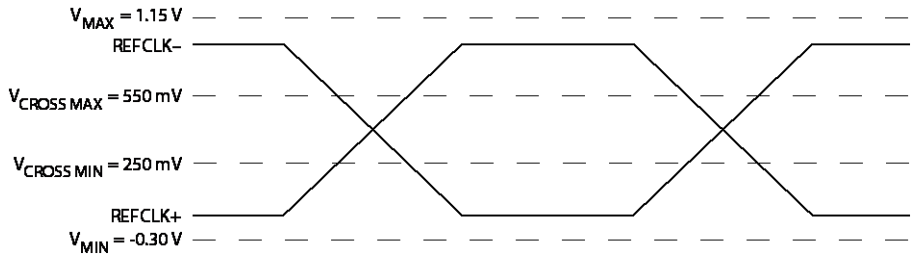


Figure 2-3. Single-Ended Measurement Points for Absolute Cross Point and Swing

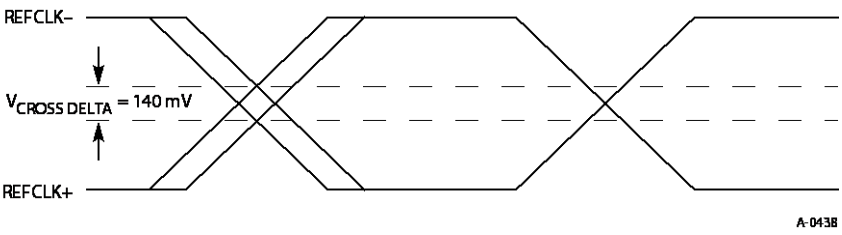


Figure 2-4. Single-Ended Measurement Points for Delta Cross Point

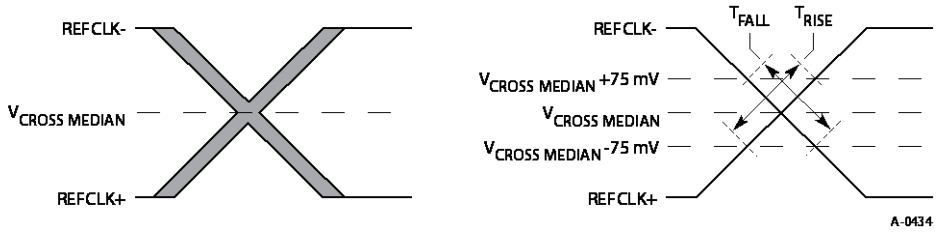


Figure 2-5. Single-Ended Measurement Points for Rise and Fall Time Matching

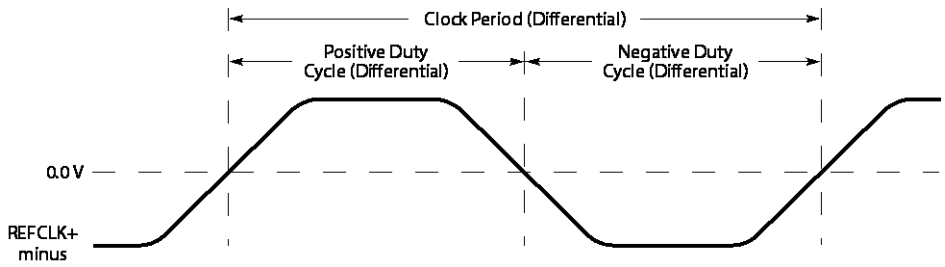


Figure 2-6. Differential Measurement Points for Duty Cycle and Period

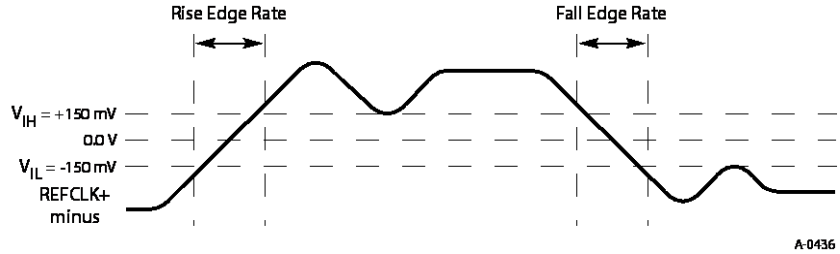


Figure 2-7. Differential Measurement Points for Rising and Falling Edge Rate

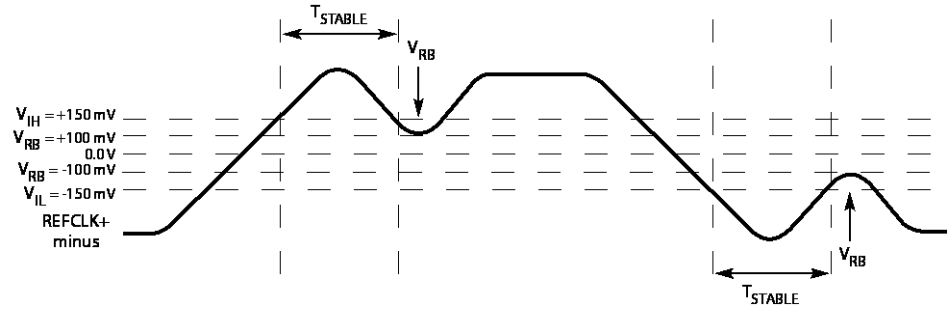


Figure 2-8. Differential Measurement Points for Ring-back

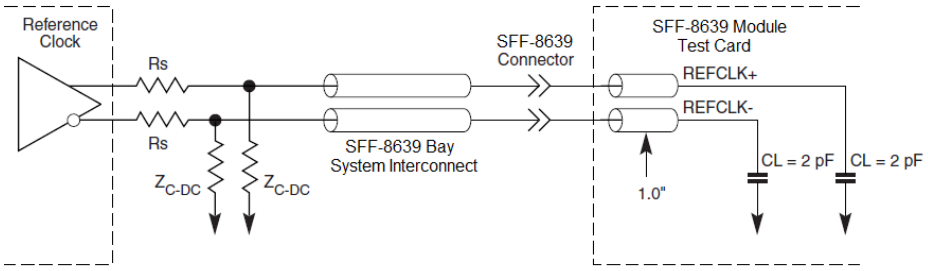


Figure 2-9. Reference Clock System Measurement Point and Loading

2.1.4. REFCLK Phase Jitter Specification for 2.5 GT/s Signaling Support

The phase jitter of the reference clock is to be measured using the following clock recovery function:

$$H(s) = \left[H_1(s) - H_2(s) * e^{-s*t\_delay}\right] \cdot H_3(s)$$

where:

$$H_1(s) = \frac{2s\zeta\omega_1 + \omega_1^2}{s^2 + 2s\zeta\omega_1 + \omega_1^2}$$

$$H_2(s) = \frac{2s\zeta\omega_2 + \omega_2^2}{s^2 + 2s\zeta\omega_2 + \omega_2^2}$$

$$H_3(s) = \frac{s}{s + \omega_3}$$

$$\zeta = 0.54$$

$$\omega_1 = \frac{2 * \pi * 22 \cdot 10^6}{\sqrt{1 + 2\zeta^2 + \sqrt{\left(1 + 2\zeta^2\right)^2 + 1}}} Rad / s$$

$$\omega_2 = \frac{2 * \pi * 1.5 \cdot 10^6}{\sqrt{1 + 2\zeta^2 + \sqrt{\left(1 + 2\zeta^2\right)^2 + 1}}} Rad / s$$

$$\omega_3 = 2 * \pi * 1.5 \cdot 10^6 \; Rad / s$$

$$t\_delay = 10 \cdot 10^{-9} \; s$$

The maximum allowed magnitude of the peak-peak reference clock jitter is given in Table 2-2. For information about the maximum peak-peak phase jitter value, refer to *PCI Express Jitter Modeling* white paper. Multiple methods are available to measure the maximum allowed peak-peak phase jitter value.

A sampling rate of 20 giga-samples per second, or better, must be used for all real-time sampling scopes. Take enough data to guarantee the proper bit error ~~rate~~ ratio (BER). Reference clock measurements for cards are taken with a differential, high-impedance probe using the circuit of Figure 2-9 at the load capacitors CL. Measurements for devices on the same board are made using a differential, high-impedance probe as close to the REFCLK+ and REFCLK- input pins as possible. The limits in Table 2-2 must be met using both the rising edges and falling edges of the reference clock in the phase jitter analysis.

Table 2-2. Maximum Allowed Phase Jitter When Applied to Fixed Filter Characteristic

BER*	Maximum Peak-Peak Phase Jitter Value (ps)
10^{-6}	86
10^{-12}	108

*Each row entry provides jitter limits at different BER values on a bathtub curve. If bathtub curves are not used in jitter measurements, then the jitter limit in the 10^{-6} row is used as the total jitter limit for measurements using approximately 10^{6} Unit Intervals of data.

2.1.5. REFCLK Phase Jitter Specification for 5.0 GT/s Signaling Support

This specification does not provide a separate reference clock jitter specification for 5.0 GT/s signaling support. Instead, a two-port methodology for simultaneously assessing the system board data and reference clock is described with specified limits given in Section 4.6.8.

2.1.6. REFCLK Phase Jitter Specification for 8.0 GT/s Signaling Support

This specification does not provide a separate reference clock jitter specification for 8.0 GT/s signaling support. In this revision of the specification, the motherboard Transmitter eye requirements include worst-case reference clock jitter of 1 ps RMS under the 8.0 GT/s reference clock requirements for common clock architecture in the *PCI Express Base Specification*.

2.2. PERST# Signal

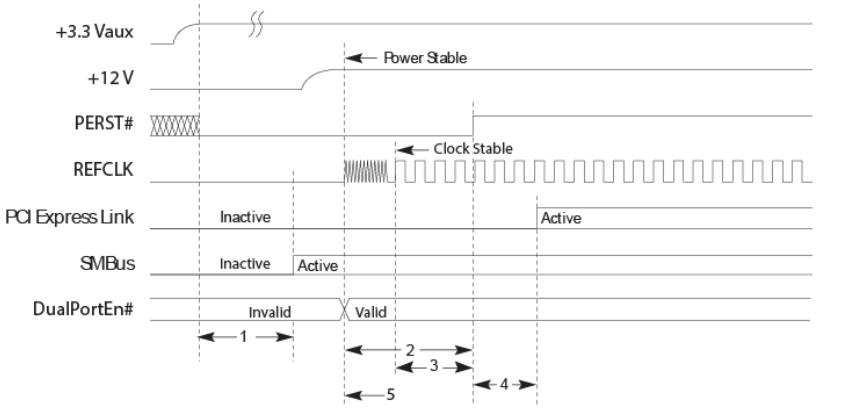
The PERST# signal is used to indicate when the power supply is within its specified voltage tolerance and is stable. It also initializes a component's state machines and other logic once power supplies stabilize. On power up, the de-assertion of PERST# is delayed a minimum of T_{PVPERL} from the power rails achieving specified operating limits. Also, within this time, the reference clocks (REFCLK+, REFCLK-) must become stable, at least $T_{PERST-CLK}$ before PERST# is de-asserted. PERST# is asserted in advance of the power being switched off in a power-managed state like S3. PERST# is asserted when the power supply is powered down, but without the advanced warning of the transition. DualPortEn# must be valid prior to the de-assertion of both PERST# and the optional PERSTB# signals.

Note: If Dual port mode is enabled, PERST# requirements apply to PERSTB#. All PCI Express reset requirements apply independently to both ports. If Dual port mode is not enabled, the assigned pin does not function as PERSTB#.

2.2.1. Initial Power-Up (G3 to S0)

When PERST# is active, all PCI Express functions are held in reset. The +12 V supply ramps up to the level specified in Table 4-1. During this stabilization time, the reference clock starts and stabilizes. After the specified time has elapsed for power (T_{PVPERL}) and clock ($T_{PERST-CLK}$) to stabilize, PERST# is de-asserted.

On initial power-up, the hardware default state of the Active State Power Management Control field in the Link Control register must be set to 00b. Only the system BIOS and operating system are permitted to change this field. Other software agents should not change this field.



1. +3.3Vaux stable to SMBus driven (optional).
2. Minimum time from power rails within specified tolerance to PERST# inactive (T_{PVPERL}).
3. Minimum clock valid to PERST# inactive ($T_{PERST-CLK}$).
4. Minimum PERST# inactive to PCI Express link out of electrical idle.
5. The system asserts DualPortEn# by driving the open drain output low. DualPortEn# is deasserted when the system permits the module to pull it high. This signl is not valid prior to power stable.

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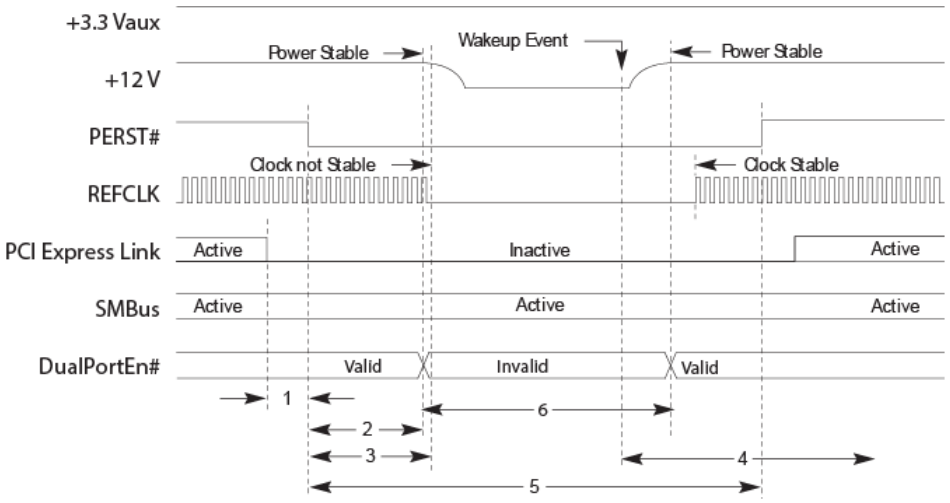
459 **Figure 2-10. Power Up**

460 2.2.2. Power Management States (S0 to S3/S4 to S0)

461 For the system to enter the S3/S4 state, devices are placed into $D3_{hot}$ states with Links in L2 (or L3
462 if +3.3 Vaux is not utilized) prior to any power transitions at the slot. The main power and reference
463 clock supplied to the SFF-8639 module will go inactive and stay inactive until a wakeup event. Upon
464 the removal of main power, devices enter the $D3_{cold}$ state. During the $D3_{cold}$ state,
465 +3.3 Vaux remains at +3.3 V. On the wakeup event, the power manager restores the main power
466 and reference clocks. As in the last section, PERST# de-asserts T_{PVPERL} after the clocks and power
467 are stable (see Figure 2-11).

468 On resume from a $D3_{cold}$ state, the hardware default state of the Active State Power Management
469 Control field in the Link Control register must be set to 00b. Only the system BIOS and operating
470 system are permitted to change this field. Other software agents must not change this field.

471



1. The PCI Express link will be put into electrical idle prior to PERST# going active.
2. PERST# goes active before the power on the connector is removed.
3. Clock and JTAG go inactive after PERST# goes active.
4. A wakeup event resumes the power to the connector, restarts the clock, and the sequence proceeds as in power up.
5. The minimum active time for PERST# is T_{PERST}.
6. The system is not permitted to change the state of DualPortEn# during $D3_{cold}$ transitions. However, DualPortEn# is only valid when power is stable.

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473 **Figure 2-11. Power Management States**

2.2.3. Power Down

The +3.3 Vaux power rail is deemed to be valid or stable if the specified voltage is within the associated voltage tolerances defined in Table 4-1. Voltage levels for a valid and stable +12 V power rail are vendor specified. Once a power rail is deemed stable, an invalid or unstable rail is defined as a rail that has dropped below the specified minimum voltage levels (for example, below 2.8 V for the +3.3 Vaux rail).

The out-of-tolerance threshold windows are shown in Figure 2-12 and power down is shown in Figure 2-13.

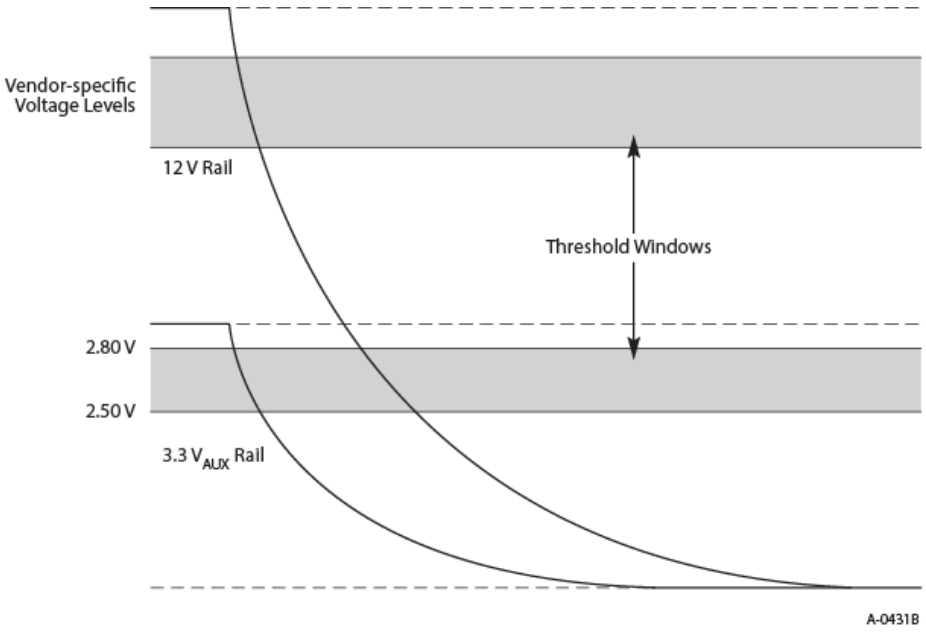
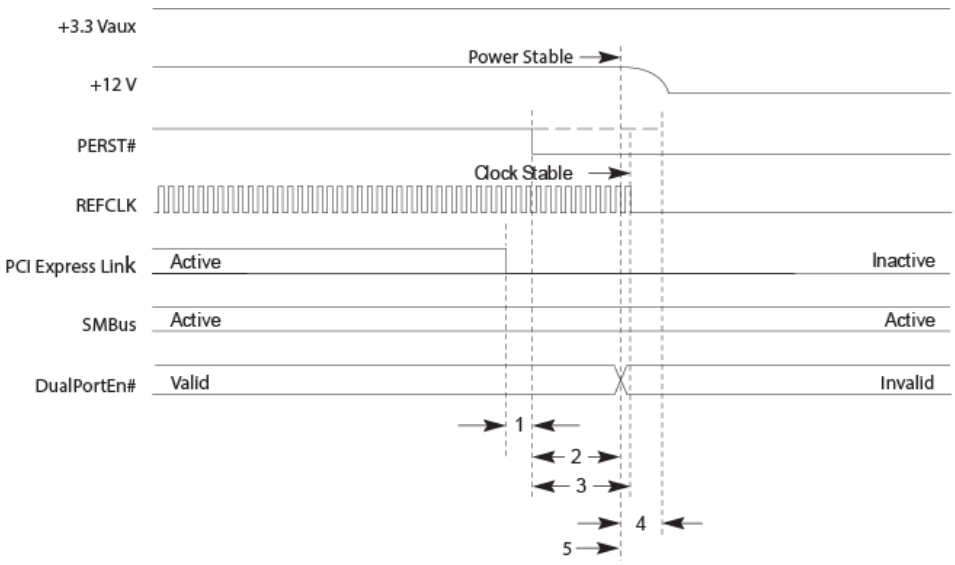


Figure 2-12. Out-of-tolerance Threshold Windows



1. The PCI Express link is not put into an inactive state (Device in $D3_{hot}$) prior to PERST#
2. PERST# goes active before the power on the connector is removed.
3. Clock goes inactive after PERST# goers active.
4. In the case of a surprise power down, PERST# goes active T_{FAIL} after power is no longer stable.
5. DualPortEn# is only valid when power is stable.

Figure 2-13. Power Down

2.3. WAKE# Signal

The WAKE# signal is an open drain, active low signal that is driven low by a PCI Express component to reactivate the main power rails and reference clocks of the SFF-8639 module bay. The WAKE# signal is used by Downstream Ports to signal to functions on the SFF-8639 module in conjunction with the OBFF mechanism. Only SFF-8639 models that support either the wakeup function process or the OBFF mechanism connect to this pin. If the SFF-8639 module has wakeup capabilities, it must support the WAKE# function. Likewise, only systems that support the wakeup function or the OBFF mechanism need to connect to this pin. Such systems are not required to support Beacon as a wakeup mechanism, but are encouraged to support it. If the wakeup function is used, the +3.3 Vaux supply must be present and used for this function. The assertion and de-assertion of WAKE# are asynchronous to any system clock. (Refer to the *PCI Express Base Specification* for more details on PCI-compatible power management.)

If the WAKE# signal is supported by an SFF-8639 module bay, the signal is connected to the platform's power management (PM) controller. WAKE# may be bused to multiple SFF-8639 bays and PCI Express Add-in Card connectors, forming a single input connection at the PM controller, or individual connectors can have individual connections to the PM controller. Hot-Plug requires that WAKE# be isolated between connectors and driven inactive during the Hot-Plug/Hot Removal events.

Auxiliary power (+3.3 Vaux) must be used by the asserting and receiving ends of WAKE# to revive the Hierarchy. The system vendor must also provide a pull-up on WAKE# with its bias voltage reference being supplied by the auxiliary power source in support of Link reactivation. Note that the voltage that the system board uses to terminate the WAKE# signal is lower than the auxiliary supply voltage to be compatible with lower voltage processes of the system PM controller. However, all potential drivers of the WAKE# signal must be +3.3 V tolerant.

WAKE# must only be asserted by the SFF-8639 module when all its functions are in the D3 state and at least one of its functions is enabled for wakeup generation using the PME Enable bit in the Power Management Control/Status Register (PMCSR) defined in the *PCI Bus Power Management Interface Specification*.

Note: WAKE# is not PME# and must not be attached to the PCI-PME# interrupt signals. WAKE# causes power to be restored, but does not directly cause an interrupt.

If the SFF-8639 module supports the OBFF mechanism defined in the *PCI Express Base Specification*, then the WAKE# signal may be used as an input to the SFF-8639 module. If Dual port mode is enabled, both the A-side and B-side ports receive the same OBFF information from the WAKE# signal. Refer to the *PCI Express Base Specification* for specifics of the OBFF mechanism.

WAKE# has additional electrical requirements over and above standard open drain signals that allow it to be shared between devices that are powered off and those that are powered on using auxiliary power, for example. The additional requirements include careful circuit design to ensure that a voltage applied to the WAKE# signal network never causes damage to a component, even if that component's power is not applied.

Additionally, the module must ensure that it does not pull WAKE# low unless WAKE# is being intentionally asserted in all cases, including when the related function is in $D3_{cold}$.

This means that any component implementing WAKE# must be designed such that:

- Unpowered WAKE# output circuits are not damaged if a voltage is applied to them from other powered wire-ORed sources of WAKE#.
- When power is removed from its WAKE# generation logic, the unpowered output does not present a low impedance path to ground or any other voltage.

These additional requirements ensure that the WAKE# signal network continues to function properly when a mixture of auxiliary powered and unpowered components have their WAKE# outputs wire-ORed together. It is important to note that most commonly available open drain and tri-state buffer circuit designs used, as is, do not satisfy the additional circuit design requirements for WAKE#.

Other requirements and recommendations for the system board/SFF-8639 module design include:

- Common ground plane reference between slots/components attached to the same WAKE# signal.
- If +3.3 Vaux is supplied to one SFF-8639 module bay or PCI Express connector in a chassis, it must be supplied to all SFF-8639 module bays and PCI Express connectors in that chassis.
- If WAKE# is supported on one SFF-8639 module bay or PCI Express connector in a chassis, it must be supported on all SFF-8639 module bays and PCI Express connectors in that chassis.
- If the system does not support +3.3 Vaux and the wakeup function, the +3.3 Vaux SFF-8639 module bay connector pin is left open. Refer to the *PCI Bus Power Management Interface Specification* for +3.3 Vaux power requirements.
- +3.3 Vaux voltage supply may be present, even if the module is not enabled for wakeup events.
- +12 V at the SFF-8639 bay may be switched off by the system.
- SFF-8639 modules are permitted to generate the Beacon wakeup mechanism, in addition to using the WAKE# mechanism, although the system is not required to provide support for Beacon.

Note: If the SFF-8639 module uses the Beacon mechanism, in addition to the WAKE# mechanism, the Beacon may be ignored by the system. Circuits that support the wakeup function and are intended to work in any PCI Express system must be designed to generate the Beacon on their PCI Express data lines.

SFF-8639 module designers must be aware of the special requirements that constrain WAKE# and ensure that their modules do not interfere with the proper operation of the WAKE# network. The WAKE# input into the system may de-assert as late as 100 ns after the WAKE# output from the function de-asserts (for example, the WAKE# pin must be considered indeterminate for a number of cycles after it has been de-asserted).

The appropriate value of the pull-up resistor for WAKE# on the system board is derived from the total possible capacitance on WAKE# to ensure that WAKE# charges up to a logic high voltage level in no more than 100 ns. (Refer to the *PCI Local Bus Specification* for additional information on pull-up resistors.)

IMPLEMENTATION NOTE

Example WAKE# Circuit Design

An example of how the WAKE# generation logic may be implemented is shown in Figure 2-14. In this example, multiple PCI Express functions have their WAKE# signals ganged together and connected to the single WAKE# pin on the SFF-8639 module connector.

The circuit driving the gate of transistor Q1 is designed to isolate the SFF-8639 bay's or Add-in Card's WAKE# network from that of the system board whenever its power source (V_{SOURCE}) is absent.

If the SFF-8639 module supplies power to its WAKE# logic derived from the SFF-8639 module bay +12 V supply (for example, it does not support wakeup from $D3_{cold}$), then all WAKE# sources from the module will be isolated from the system board when the +12 V rail at the SFF-8639 module interface is switched off. SFF-8639 modules that support wakeup from $D3_{cold}$ have an auxiliary power source (+3.3 Vaux) to power the WAKE# logic, which maintains connection of these WAKE# sources to the system board's WAKE# signal network even when the Link Hierarchy's power (+12 V) has been switched off.

The example shown in Figure 2-14 assumes that all sources of WAKE# on the SFF-8639 module are either powered by the +3.3 Vaux (V_{SOURCE}) or derived from +12 V. If WAKE# from $D3_{cold}$ is supported by some, but not all the SFF-8639 module's functions that generate WAKE#, the SFF-8639 module designer provides separate isolation control for each of the WAKE# generation power sources to ensure proper operation.

The SFF-8639 module may have the "power fail detect" isolation circuitry integrated within the WAKE# output pin corresponding to the source of FET Q1. Alternatively, all isolation control logic may be implemented externally on the SFF-8639 module.

This example provides a conceptual aid, and is not intended to prescribe an actual implementation.

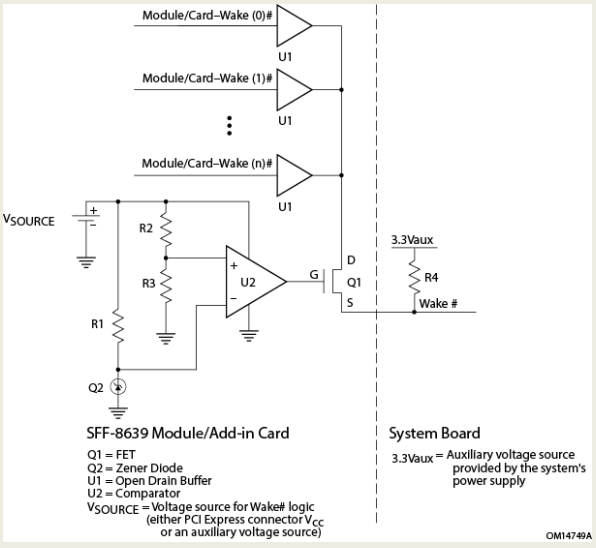


Figure 2-14. Wake Circuit

2.4. ACTIVITY# (Required)

The ACTIVITY# signal is an open drain, active low signal that indicates activity on the SFF-8639 module. The system must provide a pull-up resistor to de-assert this signal. All other details are vendor specific.

2.5. DualPortEn# (Optional)

When de-asserted, the SFF-8639 module is configured as a single x4 PCI-Express device. When asserted, the SFF-8639 module is configured as two independent x2 PCI-Express devices. As independent ports, the absence of the A-side port (or B-side port) on the system or module must not alter the operation of the other port.

Support of DualPortEn# is optional. The system asserts the open-drain signal by driving it low. Electrical characteristics are described in Table 2-4. Control signal mapping is detailed in Table 2-3. DualPortEn# is valid only when supported by both the system and module.

Table 2-3. DualPortEn# Control Signal Map

Auxiliary Signals	Dual Port Disabled	Dual Port Enabled	
	Lanes 0, 1, 2, and 3,	Lanes 0 and 1	Lanes 2 and 3
Reference Clock +	REFCLK+	REFCLK+	REFCLKB+
Reference Clock -	REFCLK-	REFCLK-	REFCLKB-
Fundamental Reset	PERST#	PERST#	PERSTB#
Wake	WAKE#	WAKE#	WAKE#
Clock Request	CLKREQ#	CLKREQ#	CLKREQ#
Interface Detect	IfDet#	IfDet#	IfDet#
Present	PRSNT#	PRSNT#	PRSNT#
Activity	ACTIVITY#	ACTIVITY#	ACTIVITY#
SMBCLK	SMBCLK	SMBCLK	SMBCLK
SMBDAT	SMBDAT	SMBDAT	SMBDAT

2.6. SMBus (Optional)

The optional System Management Bus (SMBus) is a two-wire interface through which various system component chips communicate with each other and with the rest of the system. It is based on the principles of operation of I^2C.

SMBus provides a control bus for system and power management related tasks. A system may use SMBus to pass messages to and from devices instead of tripping individual control lines. Removing the individual control lines reduces pin count. Accepting messages ensures future expandability.

With SMBus, a module may provide manufacturer information, tells the system what its model/part number is, saves its state for a suspend event, reports different types of errors, accepts control parameters, and returns its status. SMBus operation is independent of the +12 V power and reset. However, in the absence of +12 V power, some SMBus functionality may not operate properly.

SMBus is described in the *System Management Bus (SMBus) Specification*. Refer to this specification for DC characteristics and all AC timings. If the system board or SFF-8639 module supports SMBus, it should adhere to additional requirements that may be found in Chapter 8 of the *PCI Local Bus Specification*.

The system board provides pull-ups to the +3.3 Vaux rail, per the *PCI Local Bus Specification*. Components attached to these signals need to have a +3.3 V signaling tolerance.

The SMBus circuitry of the SFF-8639 module should be reset on the rising edge of the +3.3 Vaux rail independent of the +12 V rail. This enables the +3.3 Vaux rail to reset the SMBus circuitry for systems that are able to control the +3.3 Vaux rail.

2.6.1. Capacitive Load of High-power SMBus Lines

Capacitive load for each bus line includes all pin, wire, and connector capacitances. The maximum capacitive load affects the selection of the pull-up resistor or the current source to meet the rise time specifications of SMBus.

The value in the DC specifications (C_{OUT} in Table 2-4) is a recommended guideline, so that two SMBus devices may, for example, be populated on an SFF-8639 module.

2.6.2. Minimum Current Sinking Requirements for SMBus Devices

Devices in high-power segments are required to sink a minimum current of 4 mA, while maintaining the V_{OL2} (max) of 0.4 V. The requirement for a 4 mA sink current determines the minimum value of the pull-up resistor, $R_{PULL-UP}$.

2.6.3. SMBus *Back Powering* Considerations

Unpowered modules connected to the SMBus must provide protection against "back powering" the SMBus. Unpowered devices connected to high-power segments must meet leakage specifications in the *System Management Bus (SMBus) Specification*.

2.6.4. Power-on Reset

SMBus devices detect a power-on event in one of two ways:

- By detecting that power is being applied to the device
- For self-powered or always-powered devices, by detecting that the SMBus is active (clock and data lines have gone high after being low for more than 2.5 s)

2.7. CLKREQ# (Optional)

The CLKREQ# signal is an open drain, active low signal that is driven low by the SFF-8639 module to request that the PCI Express reference clock be available (active clock state), to allow the PCI Express interface to send/receive data. Refer to the *PCI Express Mini-CEM Specification* for details on the functional and electrical requirements for the CLKREQ# signal. The CLKREQ# signal is also used by the optional L1 PM Substates mechanism. In this case, CLKREQ# is asserted by either the system or module to initiate an L1 exit. Refer to the *PCI Express Base Specification* for details on the functional requirements for the CLKREQ# signal, when implementing L1 PM Substates. CLKREQ# is not supported in Dual port mode.

2.8. PWRDIS (Optional)

The PWRDIS signal is used by the SFF-8639 system to disable +12 V power to the SFF-8639 module circuitry. If the PWRDIS signal is supported by the SFF-8639 Module, then the SFF-8639 Module must:

- Allow +12 V power to be applied to the SFF-8639 Module circuitry if the PWRDIS signal is not connected on the SFF-8639 backplane receptacle;
- Allow +12 V power to be applied to the SFF-8639 Module circuitry if the PWRDIS signal is negated as defined in Table 2-6;
- Disable +12 V power applied to the SFF-8639 Module circuitry if:
  - The minimum negated hold time in Table 2-6 is met; and
  - The PWRDIS signal is asserted as defined in Table 2-6.
- Perform the actions defined for power on reset if:
  - The minimum negated hold time in Table 2-6 is met;
  - The PWRDIS signal is asserted as defined in Table 2-6; and
  - The PWRDIS signal transitions from asserted to negated.;
- Not respond to a change of the PWRDIS signal from negated to asserted or asserted to negated until the PWRDIS signal is held at the asserted or negated level for a minimum of 1 µs.
- PWRDIS removes power only to the +12 V powered circuitry.
- PWRDIS functionality must be independent of the availability of +3.3 Vaux.

Note: This approach facilitates use of single-chip I2C PROM devices, as well as other SMBus implementations, powered from +3.3 Vaux. For example, this SMBus device memory map may provide access to vital product data accessible with the application of only +3.3 Vaux power and extended management capabilities with the application of both +3.3 Vaux and +12 V power.

Implementation Note: Legacy systems may have a pull-up resistor on the system-side of the PWRDIS interface to deassert CLKREQ#. This may disable the +12 V powered circuitry of the SFF-8639 module.

2.9. Auxiliary Signal Parametric Specifications

2.9.1. DC Specifications

The DC specifications for ACTIVITY#, DualPortEn#, PERST#, WAKE#, CLKREQ#, PERSTB#, IfDet#, PRSNT#, and SMBus are given in Table 2-4.

Table 2-4. Auxiliary Signal DC Specifications - ACTIVITY#, DualPortEn#, PERST#, WAKE#, CLKREQ#, PERSTB#, IfDet#, PRSNT#, and SMBus

Symbol	Parameter	Conditions	Min	Max	Unit	Notes
V_{IL1}	Input Low Voltage		-0.5	0.8	V	2, 6
V_{IH1}	Input High Voltage		2.0	3.8	V	2, 6
V_{IL2}	Input Low Voltage		-0.5	0.8	V	4
V_{IH2}	Input High Voltage		2.1	+3.3 Vaux + 0.5	V	4
V_{OL1}	Output Low Voltage	4.0 mA		0.2	V	1, 3, 8
V_{HMAX}	Max High Voltage			3.8	V	3, 8
V_{OL2}	Output Low Voltage	4.0 mA		0.4	V	1, 4
V_{OL3}	Output Low Voltage	15.0 mA		0.2	V	1, 7
I_{in}	Input Leakage Current	0 V to +3.3 V	-10	+10	µA	2, 4
I_{lkg}	Output Leakage Current	0 V to +3.3 V	-50	+50	µA	3, 5, 8
C_{in}	Input Pin Capacitance			7	pF	2
C_{out}	Output (I/O) Pin Capacitance			30	pF	3, 4, 8
~~$R_{PULL-UP}$~~	~~Pull-Up Resistance~~		~~9~~	~~60~~	~~kΩ~~	~~9~~

Notes:

1. Open-drain output. For outputs of the SFF-8639 module, a pull-up is required on the system board. There is no V_{OH} specification for these signals. The number given is the maximum voltage allowed to be applied to this pin.
2. Applies to PERST# and PERSTB#.
3. Applies to WAKE#, CLKREQ#, IfDet#, PRSNT#, and DualPortEn#.
4. Applies to SMBus signals SMBDAT and SMBCLK.
5. Leakage at the pin when the output is not active (high impedance).
6. Applies to WAKE# issued by Switch Downstream Ports and Root Complex for signaling of OBFF indications, as received at the input of the Endpoint(s).
7. Applies to ACTIVITY#. Open-drain output of SFF-8639 module to activate LED with series bias resistor. LED and series bias resistor are external to the SFF-8639 module.
8. Open-drain output. For outputs of the system, a pull-up is required on the SFF-8639 module.
9. ~~Applies to CLKREQ#, IfDet#, and PRSNT# pull-ups on the system side and DualPortEn# pull-up on the module side~~.

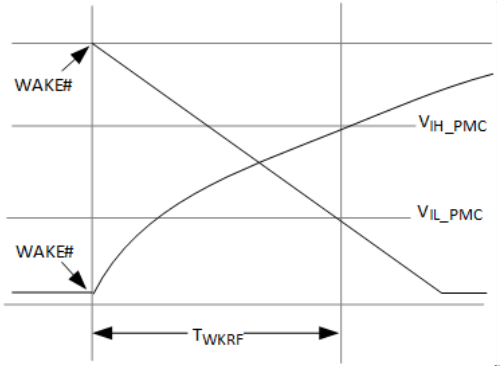
2.9.2. AC Specifications

The power sequencing and reset signal timings are given in Table 2-5 and the WAKE# Rise and Fall time measurement points are shown in Figure 2-15.

Table 2-5. Power Sequencing and Reset Signal Timings

Symbol	Parameter	Min	Max	Unit	Note	See Figure
T_{PVPERL}	Power stable too PERST# inactive	100		ms	1	Figure 2-10
$T_{PERST-CLK}$	Reference clock stable before PERST# inactive	100		µs	2	Figure 2-10
T_{PERST}	PERST# active time	100		µs		Figure 2-11
T_{FAIL}	Power level invalid to PERST# active		500	ns	3	Figure 2-13
T_{WKRF}	WAKE# rise – fall time		100	ns	4	Figure 2-15
$T_{WAKE-TX-MIN-PULSE}$	Minimum WAKE# pulse width; applies to both active-inactive-active and inactive-active-inactive cases	300		ns	5	
$T_{WAKE-FALL-FALL-CPU-ACTIVE}$	Time between two falling WAKE# edges, when signaling CPU Active	700	1000	ns	5	

Notes:
1. Any supplied power is stable when it meets the requirements specified for that power supply.
2. A supplied reference clock is stable when it meets the requirements specified for the reference clock. The PERST# signal is asserted and de-asserted asynchronously with respect to the supplied reference clock.
3. The PERST# signal must be asserted within T_{FAIL} of any supplied power going out of specification.
4. Measured from WAKE# assertion/de-assertion to valid input level at the system PM controller. Since WAKE# is an open-drain signal, the rise time is dependent on the total capacitance on the platform and the system board pull-up resistor. It is the responsibility of the system designer to meet the rise time specification.
5. Refers to timing requirement for indicating an active window.



Note: V_{IH_PMC} is the power management controller high input switching level and V_{IL_PMC} is the power management controller low input switching level. Both values are platform dependent and outside the scope of this specification.

Figure 2-15. WAKE# Rise and Fall Time Measurement Points

Commented [TS1]: Note from Excel Comment List: SFF Connector spec must have its own picture. The CEM is different.

2.9.3. PWRDIS Electrical Characteristics

The PWRDIS DC and AC electrical characteristics are provided in Table 2-6.

Table 2-6. PWRDIS DC and AC Electrical Characteristics Applied to the SFF-8639 Module

Parameter	Min	Max	Unit	Note
Absolute maximum input voltage range	-0.5	3.6	V	
Negated voltage (power enabled)	-0.5	0.7	V	1
Asserted voltage (power disabled)	2.1	3.6	V	2
Driver sink/source current capability	~~100~~1		~~µ~~mA	1 and 2
POWER DISABLE asserted hold time	5.0		s	3 and 4
POWER DISABLE negated hold time	30.0		s	3 and 4

Notes:
1. The PWRDIS signal should be actively negated. If the PWRDIS signal is not actively negated (e.g. open), then the specified values for the PWRDIS signal negated voltage and driver sink current capability applied to the SFF-8639 module do not apply.
2. The PWRDIS signal must be actively asserted.
3. The hold time is the length of time the PWRDIS signal is asserted or negated. The length of time after the PWRDIS ~~DWRDIS~~ signal is asserted or negated until the disabling or allowing of power application to the SFF-8639 module circuitry is vendor specific.
4. The PWRDIS signal should not transition from negated to asserted or asserted to negated for the negated hold time:
   - After power is applied to the SFF-8639 backplane receptacle, or
   - After the detection of a hot plug event

678

3

679 # 3. Hot Insertion and Removal

680 In this chapter, all references to mechanical elements are interpreted in the context of the SFF-8639
681 module form factor definition, unless otherwise stated.

682 ## 3.1. Scope

683 The *PCI Express Base Specification* natively supports Hot-Plug/Hot Removal. However, hardware
684 support of Hot-Plug/Hot Removal of the SFF-8639 module is optional. The PCI Express Native
685 Hot-Plug model is based on the standard usage model defined in Chapter 5.

686 This chapter describes Hot-Plug/Hot Removal of the SFF-8639 connector interface on the SFF-
687 8639 module. Hot-Plug/Hot Removal of other connector interfaces within the SFF-8639
688 system/module topology is outside the scope of this specification. Physical alignment for all Hot-
689 Plug applications must ensure the mating sequence specified in *SFF-8639: Multifunction 6X Unshielded*
690 *Connector*. For a detailed explanation of the register requirements and standard usage model, refer to
691 the *PCI Express Base Specification*.

692 ## 3.2. Hot Removal Detection

693 The SFF-8639 interface includes the PRSNT# and IfDet# signals, as an out of band presence detect
694 mechanism, to detect the presence of the SFF-8639 module. Since PRSNT# and IfDet# are not in
695 the last-to-mate and first-to-break group, another vendor-specific mechanism is required to provide
696 warning of module removal. The REFCLK+, REFCLK-, REFCLKB+, REFCLKB-, PERST#,
697 PERSTB#, and SMBus signals are not required when the module is not present. In addition,
698 REFCLKB+, REFCLKB-, and PERSTB# signals are not required when DualPortEn# is disabled.
699 The two signals, PRSNT# and IfDet#, are required on the SFF-8639 bay connector and must be
700 supported by all SFF-8639 modules. The mating sequence of all SFF-8639 pins is provided in
701 Chapter 5 of this document.

702 Presence of the SFF-8639 module is indicated by simultaneous assertion of the active low IfDet#
703 signal and de-assertion of the SFF-8639 PRSNT# signals. Absence of the SFF-8639 module is
704 indicated by de-assertion of both the IfDet# and PRSNT# signals. All other state combinations of
705 these two signals are outside the scope of this specification.

Design of the system-side interface logic and signal levels for PRSNT# and IfDet# and associated use of applicable Hot-Plug control logic is vendor specific.

The PRSNT# pin of the module must be left open. The system must provide a pull-up resistor to +3.3 V to de-assert this signal (see Table 2-4).

The IfDet# pin of the module must be connected to ground. The system must provide a pull-up resistor to +3.3 V to de-assert this signal (see Table 2-4).

3.2.1. Hot Insertion Detection

Once full insertion of the SFF-8639 module is detected, the SFF-8639 system must enable the Auxiliary signals: REFCLK+, REFCLK-, PERST#, SMBDAT, SMBCLK, and if Dual Port mode is active, REFCLKB+, REFCLKB-, and PERSTB#. It is the responsibility of the Root Complex or the Switch to determine the presence of the SFF-8639 module and set the presence detect bits in the appropriate register as described in the *PCI Express Base Specification*.

720

4

721 # 4. Electrical Requirements

722 Power delivery requirements defined in this chapter apply not only to SFF-8639 modules, but also to
723 the SFF-8639 bay and system.

724 ## 4.1. Power Supply Requirements

725 All SFF-8639 bays require one power rail: +12 V, with a second, optional +3.3 Vaux rail. Systems
726 that provide SFF-8639 bays are required to provide the +12 V rail to every SFF-8639 bay in the
727 system. If a system provides +3.3 Vaux to one SFF-8639 bay, the +3.3 Vaux rail must be supplied to
728 all SFF-8639 bays. In addition, as described in Chapter 2, *Auxiliary Signals*, if the platform with the
729 PCI Express interface supports the WAKE# signal, the +3.3 Vaux rail (as well as the WAKE#
730 signal) must be supplied to all SFF-8639 bays. To access the SMBus devices on the module,
731 +3.3 Vaux must be provided.

732 Table 4-1 provides the required specifications for the power supply rails available at the SFF-8639 bays.

733 **Table 4-1. Power Supply Rail Requirements**

Parameter	Description	Value
P_{max}	Maximum power[4]	25 W (max)
$P_{init\text{-}limit}$	Initial slot power limit	10 W (max)
+12 V_{tol}	Voltage tolerance (at pin)[5]	-
+12 V_{amp}	Max continuous current[1]	2.45 A (max)
+12 $V_{peak\text{-}amp}$	Max peak current[2]	4.5 A (max)
+12 $V_{ramp\text{-}amp}$	Max power-up ramp current[3]	2 A (max)
+12 V_{drop}	Voltage drop across connector	80 mV (max)
+3.3 $VAux_{tol}$	Voltage tolerance (at pin)	±15 % (max)
+3.3 $VAux_{amp}$	Max continuous current[1]	~~20 µA~~1 mA (SMBus inactive) ~~1~~ 5 mA (SMBus or +12 V active)
+3.3 $VAux_{cap}$	Max cap load[6]	5 µF (max)
SMBus delay	Delay from ~~+12 V or~~ +3.3 Vaux power valid to SMBus ready	20 ms (min), 1.0 s (max)
	Delay from +12 V power valid to vital product data available.	20 ms (min), 1.0 s (max)
	Delay from PRSNT# and IfDet# active to SMBus ready	20 ms (min), 1.0 s (max)

Notes:
1. Maximum continuous current is defined as the highest averaged current value over any one second period.
2. Maximum current, to limit connector damage and instantaneous power.
3. Maximum current load presented by the SFF-8639 module on the power rail of the SFF-8639 receptacle during the initial power-up ramp to 90% of the minimum SFF-8639 module operating voltage.
4. Configured by the Slot Capabilities register, defined in the *PCI Express Base Specification*.
5. Vendor specific. No tolerance specified.
6. Maximum capacitance presented by the SFF-8639 module on the power rail at the SFF-8639 receptacle.

734

735 # 4.2. Power Supply Sequencing

736 There is no specific requirement for power supply sequencing of either power rail. The system,
737 however, must assert the PERST# signal, and if operating in dual port mode the PERSTB# signal,
738 whenever the +12 V power rail goes outside of the specifications provided in Table 4-1 (see Section
739 2.2 for specific information on the function and proper use of the PERST# and PERSTB# signals).

4.3. Power Supply Decoupling

Due to the low level signaling of the PCI Express interface, it is strongly recommended that sufficient decoupling of all power supplies be provided. This is recommended to ensure that power supply noise does not interfere with the recovery of data from a remote Upstream PCI Express device.

Note: It is the responsibility of the SFF-8639 module designer to properly test the design to ensure that module circuitry does not create excessive noise on power supply or ground signals at the module connector interface.

4.4. Electrical Topologies and Link Definitions

The remainder of this chapter describes the electrical characteristics of SFF-8639 modules. The electrical characteristic at the module interface is defined in terms of electrical budgets. This budget allocation decouples the electrical specification for the system designer and the module vendor and ensures successful communication between the PCI Express signal input and output Links at the SFF-8639 bay and module interface. The signaling rate for encoded data is 8.0 GT/s, 5.0 GT/s, or 2.5 GT/s and the signaling is point-to-point. Requirements are called out separately for 8.0 GT/s, 5.0 GT/s, and 2.5 GT/s signaling rates. SFF-8639 bays and modules that support the 5.0 GT/s rate must also support the 2.5 GT/s rate. SFF-8639 bays and modules that support the 8.0 GT/s rate must also support the 5.0 GT/s and 2.5 GT/s rates.

4.4.1. Topologies

Three possible electrical topologies for SFF-8639 implementations include:

- PCI Express devices across one connector in a system with a system board and an SFF-8639 module
- PCI Express devices across two connectors in a system with a system board, cable and an SFF-8639 module
- PCI Express devices across three connectors in a system with a system board, cable, backplane, and an SFF-8639 module

The topology of "SFF-8639 module on system board" allows an SFF-8639 module to be directly connected to a system board with only the SFF-8639 connector interface (Figure 4-1). In this topology, only one connector interface exists.

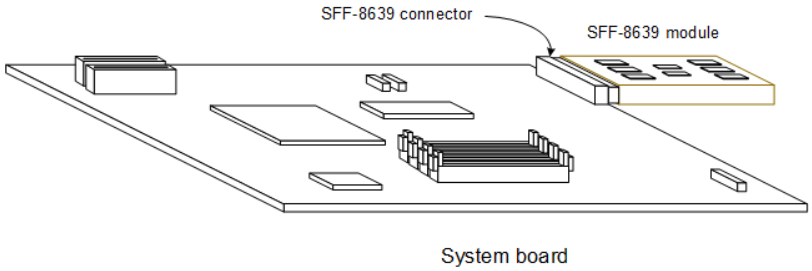


Figure 4-1. SFF-8639 Module on System Board

The topology of SFF-8639 module cabled to system board allows for an SFF-8639 module to be directly connected to a system board with a cable (Figure 4-2). In this topology, one end of the cable connects to the SFF-8639 module and the other end to the system board, using a connector interface outside the scope of this specification.

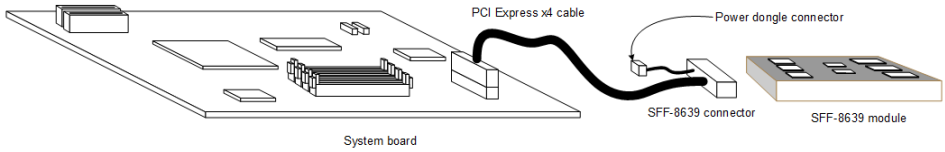


Figure 4-2. SFF-8639 Module Cabled to System Board

The topology of SFF-8639 module connected with backplane and cable allows for an SFF-8639 module to be connected to a backplane with a cable connecting the system board to the backplane (Figure 4-3). The cable connectors are outside the scope of this specification. In this topology, three connector interfaces exist.

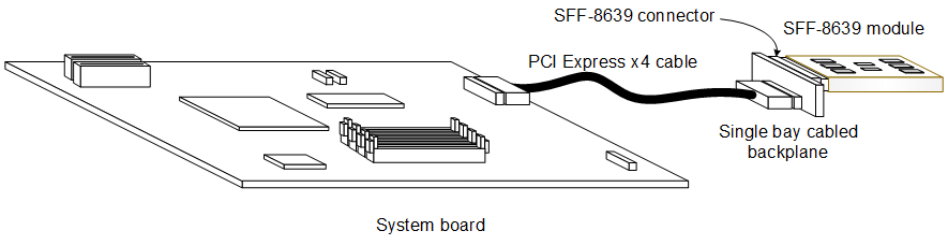


Figure 4-3. SFF-8639 Module Connected with Backplane and Cable

4.4.2. Link Definition

Typical PCI Express Links consist of the following:

- Transmitters/Receivers on an ASIC on a system board or Switch
- Package fan-in and fan-out trace topologies
- PCB-coupled microstrip and/or striplines
- Vias for layer changes
- Optional proprietary cables with connectors
- Optional proprietary backplanes with connectors
- Optional proprietary backplane with microstrip and/or stripline trace
- Coupled microstrip line and/or stripline traces on SFF-8639 module
- AC-coupling capacitors
- Transmitter/Receivers on an ASIC on the SFF-8639 module

The electrical parameters for the Link are subdivided into two components (as shown in Figure 4-4):

- SFF-8639 module
- System board and mated SFF-8639 connector (and cable, or cable + backplane, if it exists)

The electrical impact of discontinuities on the Link, such as vias, bends, and test-points, must be included in the respective components.

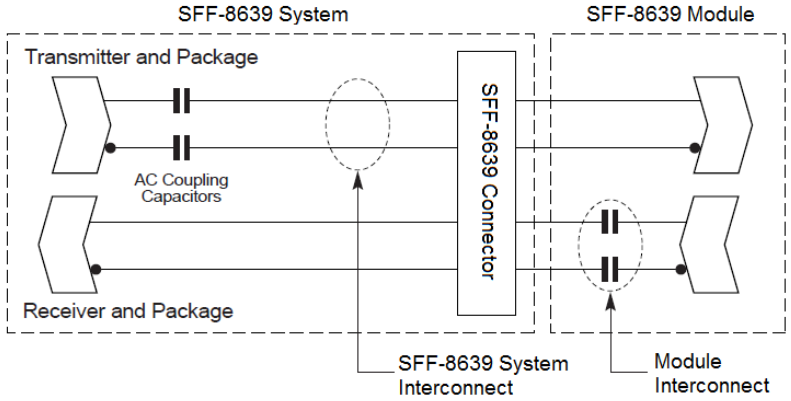


Figure 4-4. Link Definition for Two Components

4.5. Electrical Budgets

A budget is defined for each of the following electrical parameters associated with the Link:

- AC-coupling capacitors
- Insertion Loss (Voltage Transfer Function)
- Jitter
- Lane-to-Lane skew
- Crosstalk
- Equalization
- Skew within a differential pair
- Differential data trace impedance
- Differential data trace propagation delay

The electrical budgets are different for each of the two Link components:

- SFF-8639 module budget
- System board, backplane, cable and mated SFF-8639 connector budgets, where applicable

The interconnect Link budget allocations associated with the Transmitters and Receivers differ. This is to account for any electrical characteristics the AC-coupling capacitors may contribute to the Link.

4.5.1. AC-Coupling Capacitors

The SFF-8639 module and system board must incorporate AC-coupling capacitors on the Transmitter differential pair. This is to ensure blocking of the DC path between the module and the system board. The specific capacitance values are specified in the *PCI Express Base Specification*.

Capacitance value requirements are different for 8.0 GT/s data rates. Attenuation or jitter caused by the coupling capacitors must be accounted for as part of the budget allocation for the physical interconnect component's path on which the capacitors are mounted.

4.5.2. Insertion Loss Values (Voltage Transfer Function)

Maximum insertion loss assumptions made in computing the 2.5 GT/s eye diagram requirements are provided in the informational Appendix A.

4.5.3. Jitter Values

The maximum jitter values in terms of percentage of Unit Interval (UI = 400 ps for 2.5 GT/s, UI = 200 ps for 5.0 GT/s, and UI = 125 ps for 8.0 GT/s) are specified for the system board and the SFF-8639 module. The jitter associated with the mated SFF-8639 connector interface and additional proprietary components such as cables or backplanes will be part of the system board jitter budget. The jitter values are defined with respect to 100 Ω differential termination, realized as two 50 Ω resistances. These resistances are referenced to ground at the interface (see Figure 4-5).

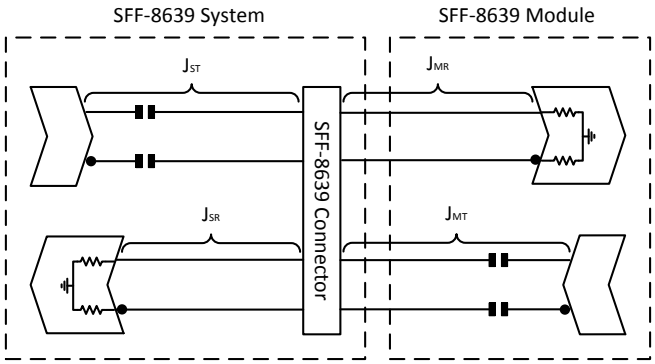


Figure 4-5. Jitter Budget

The total system jitter budget is derived with the assumption of a minimum random jitter (Rj) for each of the four budget items (Table 4-2). This minimum Rj component is used to determine the overall system budget. The probability distribution of the Rj component is at the ~~Bit Error Rate (~~BER~~)~~ indicated and is Gaussian.

For any jitter distribution, the total jitter (Tj) must always be met at the BER. The Rj of the components are independent and convolve as the root sum square. Tradeoffs of Rj and deterministic jitter (Dj) are allowed, provided the total Tj is always met. Refer to the *PCI Express Jitter and BER* for more information on the calculation of the system budget.

853 **Table 4-2. Total System Jitter Budget for 2.5 GT/s Signaling**

Jitter Contribution	Min Rj (ps)	Max Dj (ps)	Tj at BER 10^{-12} (ps)	Tj at BER 10^{-6} (ps)
Transmitter	2.8	60.6	100	87
Ref Clock	4.7	41.9	108	86
Media	0	90	90	90
Receiver	2.8	120.6	160	147
Linear Total Tj:			458	410
Root Sum Square (RSS) Total Tj:			399.13	371.52

Notes:

1. The RSS equation for the Tj at BER 10^{-12} column is Tj = $\sum Dj_n$ + 14.069 * $\sqrt{\sum Rj_n^2}$
2. The RSS equation for the Tj at BER 10^{-6} column is Tj = $\sum Dj_n$ + 9.507 * $\sqrt{\sum Rj_n^2}$
3. The Tj at BER 10^{-6} column provides jitter limits at different BER values on a bathtub curve. If bathtub curves are not used in jitter measurements, then the jitter limit in the 10^{-6} column is used as the total jitter limit for measurements using approximately 10^6 unit intervals of data.

854

855 **Table 4-3. Allocation of Interconnect Jitter Budget for 2.5 GT/s Signaling**

Jitter Parameter	Jitter Budget Value (UI)		Notes
SFF-8639 Module	J_{MR} < 0.0575	J_{MT} < 0.0650	1, 2
SFF-8639 System Board and SFF-8639 Interconnect	J_{ST} < 0.1675	J_{SR} < 0.1600	1, 3
Total Jitter	**J_T < 0.225**		**1**

Notes:

1. All values are referenced to 100 Ω, realized as two 50 Ω resistances. The jitter budget values include all possible crosstalk impacts (near-end and far-end) and potential mismatch of the actual interconnect with respect to the 100 Ω reference load.
   The *PCI Express Base Specification* allows an interconnect jitter budget of 0.225 UI (equivalent to 90 ps for a 400 ps Unit Interval). The allocated jitter budget values in Table 4-2 and Table 4-3 directly correlate to the eye diagram widths in Section 4.6. Tradeoffs in terms of attenuation, crosstalk, and mismatch are made within the budget allocations specified. No additional guard band is specifically allocated.
   The jitter allocations are then assumed per differential pair according to the table. These allocation assumptions must also include any effects of far-end crosstalk.
2. All values are referenced to 100 Ω. The SFF-8639 module budget does not include the SFF-8639 connector. However, it does include potential jitter from the AC-coupling capacitors on the Transmitter (TX) interconnect of the module. The budget allocations generally allow for a maximum of four-inch trace lengths for differential pairs having an approximate 0.127 mm (5 mil) trace width. No specific trace geometry, however, is explicitly defined in this specification. The subscripts of the symbol designators, T and R, represent the Transmitter and Receiver, respectively.
3. All values are referenced to 100 Ω. The system budget includes the mated SFF-8639 connector interface. See Section 5.2 for specifics on the standalone SFF-8639 connector budget. The system budget includes potential jitter from the AC-coupling capacitors on the Transmitter (TX) interconnect on the system board. The subscripts of the symbol designators, T and R, represent the Transmitter and Receiver, respectively.

856 The total system jitter budget for 5.0 GT/s signaling specifies separate Rj and Dj limits for each of
857 the four components in the jitter budget (Table 4-4). Refer to the *PCI Express Base Specification* for a
858 more detailed discussion of the system jitter budget, Rj and Dj.

859 **Table 4-4. Total System Jitter Budget for 5.0 GT/s Signaling**

Jitter Contribution	Max RMS Rj (ps)	Max Dj (ps)	Tj at BER 10^{-12} (ps)
Transmitter	1.4	30	50
Ref Clock	3.1	0	43.6
Media	0	58	58
Receiver	1.4	60	80
		Linear Total Tj:	231.6
		Root Sum Square (RSS) Total Tj:	200

Notes:

RSS equation for BER 10^{-12} Tj = $\sum Dj_n + 14.069 * \sqrt{\sum Rj_n^2}$

860

861 The total system jitter budget for 8.0 GT/s signaling does not set separate Rj and Dj limits for all of
862 the four components in the jitter budget. Refer to the *PCI Express Base Specification* for a more
863 detailed discussion of the system jitter budget at 8.0 GT/s.

864

Note: The jitter budget distributions above are used to derive the eye diagram widths, as described later in this chapter. However, they are provided here only as a design guideline. Compliance measurements must actually be verified against the eye diagrams themselves (see Section 4.6).

865

866 ## 4.5.4. Crosstalk

867 All SFF-8639 module designs must properly account for any crosstalk that may exist among the
868 various pairs of differential signals. Crosstalk is either near-end (NEXT) or far-end (FEXT). Each
869 component has potential impact on a design and must be planned for accordingly.

870 The minimum Electrical Idle Detect Threshold specified in the *PCI Express Base Specification* is
871 65 mV for all date rates. The Receiver tolerates crosstalk and noise up to Electrical Idle Detect
872 Threshold.

873 The system accounts for the crosstalk on the system board, mated SFF-8639 connector interface, and
874 proprietary portions of the interconnect, such as cables and backplanes (see Section 5.2).

4.5.5. Lane-to-Lane Skew

The skew at any point is measured using zero crossings of differential voltage of the compliance pattern, while simultaneously transmitting on all Physical Lanes. The compliance pattern is defined in the *PCI Express Base Specification*.

Table 4-5. Allowable Interconnect Lane-to-Lane Skew

Skew Parameter	Symbol	Skew Values	Comments
Total Interconnect Skew	S_T	1.6 ns	This does not include Transmitter output skew, $L_{TX-SKEW}$ (specified in the *PCI Express Base Specification*). The total skew at the Receiver (S_T + $L_{TX-SKEW}$) is smaller than $L_{RX-SKEW}$ (specified in the *PCI Express Base Specification*) to minimize latency.
SSF-8639 module	S_M	0.35 ns	Estimates about a 2-inch trace length delta on FR4 boards.
System Interconnect	S_S	1.25 ns	Estimates about a 7-inch trace length delta on FR4 boards.

4.5.6. Transmitter Equalization

To reduce ISI, 3.5 dB (±0.5 dB) Transmitter de-emphasis is required for 2.5 GT/s signaling. For 5.0 GT/s signaling rates, 6.0 dB (±0.5 dB) or 3.5 dB (±0.5 dB) Transmitter de-emphasis is required. For implementation details, refer to the *PCI Express Base Specification*. For SFF-8639 modules or system boards that support 8.0 GT/s signaling, refer to the *PCI Express Base Specification* for equalization preset requirements. The SFF-8639 system (the Root Complex/Switch and all interconnect up to the mated SFF-8639 connector interface) must meet eye diagram requirements given in Section 4.6, at 8.0 GT/s on each Lane, with one or more preset equalization settings.

If the equivalent of the pseudo package loss (ps21TX) parameter defined in the *PCI Express Base Specification*, measured at the end of the 5.0 GT/s SFF-8639 System Test Channel without de-embedding, shows a loss of more than 12 dB, the Root Complex/Switch initial Transmitter preset at 8.0 GT/s must be P7 or P8. Otherwise, the Root Complex/Switch initial Transmitter preset at 8.0 GT/s must be P1, P7 or P8.

If the interconnect loss from the Root Complex/Switch to the SFF-8639 connector is 12 dB or greater, then the SFF-8639 module must receive with a BER of at least 10^{-4} at 8.0 GT/s with presets P7, and P8. Otherwise the SFF-8639 module must receive with a BER of at least 10^{-4} at 8.0 GT/s with presets P1, P7 and P8.

4.5.7. Skew within the Differential Pair

The skew within the differential pair gives rise to a common-mode signal component, which can, in turn, increase Electromagnetic Interference (EMI). The differential pair traces must be routed such that the skew within differential pairs is less than 0.127 mm (5 mil) for the SFF-8639 module and 0.254 mm (10 mil) for the remaining applicable system interconnect.

4.5.8. Differential Data Trace Impedance

The PCB trace pair differential impedance for a 5.0 GT/s capable data pair must be in the range of 68 Ω to 105 Ω. The PCB trace pair differential impedance for an 8.0 GT/s capable data pair must be in the range of 70 Ω to 100 Ω. These limits apply to both the SFF-8639 module and the SFF-8639 system interconnect. This requirement does not apply to vias, the connectors, package traces, cables, and other similar structures.

IMPLEMENTATION NOTE

The PCB trace impedance requirement specified in Section 4.5.8 only applies to topologies supporting 5.0 GT/s or 8.0 GT/s, using this form factor.

4.5.9. Differential Data Trace Propagation Delay

The propagation delay for an SFF-8639 module data trace from the SFF-8639 connector footprint to the Receiver/Transmitter must not exceed 750 ps.

4.6. Eye Diagrams at the SFF-8639 Interface

The eye diagrams defined in this section represent the compliance eye diagrams that must be met for both the SFF-8639 module and system interconnect + system board interfacing with such an SFF-8639 module. The specific measurement requirements (probe test points, calibrated system interconnect + system board specifics, etc.) for compliance of physical components are outside the scope of this specification. Review of the *PCI Express Architecture PHY Test Specification* document may be beneficial. A sample size of 10^6 UI is assumed for the eye diagram measurements. These compliance eye diagrams with BER of 10^{-12} are also used for simulation by following the guidelines explained in Section 4.5.

4.6.1. SFF-8639 Module Transmitter Path Compliance Eye Diagram at 2.5 GT/s

The eye diagrams for the SFF-8639 modules Transmitter path compliance at 2.5 GT/s are defined in Table 4-6 and Figure 4-6.

Table 4-6. SFF-8639 Module Transmitter Path Compliance Eye Requirements at 2.5 GT/s

Parameter	Min	Max	Unit	Notes
V_{TXA}	514	1200	mV	1, 2, 5
V_{TXA_d}	360	1200	mV	1, 2, 5
T_{TXA}	287		ps	1, 3, 5
$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$		56.5	ps	1, 4, 5

Notes:

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires transmission of the Compliance Pattern in 8b/10b Encoding (refer to the *PCI Express Base Specification*) during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.
3. T_{TXA} is the minimum eye width. The sample size for this measurement is 10^6 UI. This value is able to be reduced to 274 ps for simulation purposes at BER 10^{-12}.
4. $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum median-to-max jitter outlier as defined in the *PCI Express Base Specification*. The sample size for this measurement is 10^6 UI. This value is able to be increased to 63 ps for simulation purposes at BER 10^{-12}.
5. The values in this table are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the SFF-8639 connector footprint on the SFF-8639 module (see Figure 4-5). The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PCI Express Architecture PHY Test Specification* document.

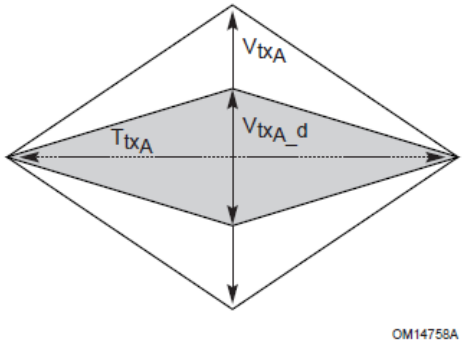


Figure 4-6. SFF-8639 Module Transmitter Path Compliance Eye Diagram

4.6.2. SFF-8639 Module Transmitter Path Compliance Eye Diagrams at 5.0 GT/s

The eye diagrams for the SFF-8639 module's Transmitter path compliance at 5.0 GT/s are defined in Table 4-7, Table 4-8, Table 4-9, Table 4-10, and Figure 4-6.

Table 4-7. SFF-8639 Module Transmitter Path Compliance Eye Requirements at 5.0 GT/s for a Link that Operates with 3.5 dB

Parameter	Min	Max	Unit	Notes
V_{TXA}	380	1200	mV	1, 2, 4
V_{TXA_d}	380	1200	mV	1, 2, 4
T_{TXA} (with crosstalk)	123		ps	1, 3, 4
T_{TXA} (without crosstalk)	126		ps	

Notes:

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires transmission of the Compliance Pattern in 8b/10b Encoding (refer to the *PCI Express Base Specification*) during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.
3. T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least 10^6 UI. The calculated eye width at BER 10^{-12} must not exceed T_{TXA}.
4. The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind an SFF-8639 connector. This channel must be referenced as the 5.0 GT/s SFF-8639 Module Test Channel. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PCI Express Architecture PHY Test Specification* document.

The SFF-8639 module Tj for the Transmitter + Transmitter interconnect must meet the requirements in Table 4-8 when decomposed into Rj and Dj.

Table 4-8. SFF-8639 Module Jitter Requirements at 5.0 GT/s for a Link that Operates with 3.5 dB

	Max Rj (ps RMS)	Max Dj (ps)	Tj at BER 10^{-12} (ps)
With crosstalk	1.4	57	77
Without crosstalk	1.4	54	74

944 **Table 4-9. SFF-8639 Module Transmitter Path Compliance Eye**
945 **Requirements at 5.0 GT/s for a Link that Operates with 6.0 dB**

Parameter	Min	Max	Unit	Notes
V_{TXA}	306	1200	mV	1, 2, 4
V_{TXA_d}	260	1200	mV	1, 2, 4
T_{TXA} (With crosstalk)	123		ps	1, 3, 4
T_{TXA} (Without crosstalk)	126		ps	

Notes:

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires transmission of the Compliance Pattern in 8b/10b Encoding (refer to the *PCI Express Base Specification*) during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.
3. T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least 10^6 UI. The calculated eye width at BER 10^{-12} must not exceed T_{TXA}.
4. The values in this table are measured using the 5.0 GT/s SFF-8639 Module Test Channel. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PCI Express Architecture PHY Test Specification* document.

946

947 The SFF-8639 module total jitter for the Transmitter + Transmitter interconnect must meet the
948 requirements in Table 4-10 when decomposed into random and deterministic jitter.

949 **Table 4-10. SFF-8639 Module Jitter Requirements at 5.0 GT/s for a Link**
950 **that Operates with 6.0 dB**

	Max Rj (ps RMS)	Max Dj (ps)	Tj at BER 10^{-12} (ps)
With crosstalk	1.4	57	77
Without crosstalk	1.4	54	74

951 ### 4.6.3. SFF-8639 Module Transmitter Path Compliance
952 ### Eye Diagrams at 8.0 GT/s

953 The eye diagrams for the SFF-8639 module's Transmitter path compliance at 8.0 GT/s are defined
954 in Table 4-11 and Figure 4-6. The SFF-8639 module must pass the eye diagram requirements with at
955 least one of the Transmitter equalization presets defined in the *PCI Express Base Specification*. The eye
956 diagram requirements are evaluated after the behavioral clock data recovery (CDR) and the
957 behavioral Receiver Equalization Algorithm, both defined in the *PCI Express Base Specification,* are
958 applied.

959 **Table 4-11. SFF-8639 Module Transmitter Path Compliance Eye**
960 **Requirements at 8.0 GT/s**

Parameter	Min	Max	Unit	Notes
V_{TXA}	34	1200	mV	1, 2, 4
V_{TXA_d}	34	1200	mV	1, 2, 4
T_{TXA}	41.25		ps	1, 3, 4

Notes:

1. A worst-case reference clock with 1 ps RMS jitter is assumed for this revision of the specification. All Links are assumed active while generating this eye diagram. The eye diagram requires transmission of the Compliance Pattern in 128b/130b Encoding (refer to the *PCI Express Base Specification*) during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. For lab use, an informative voltage limit (V_{TXA} and V_{TXA_d}) at a BER of 10^{-6} is 46 mV.
3. T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least 10^6 UI. The calculated eye width at BER 10^{-12} must not exceed T_{TXA}.
4. The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel, consisting of 14.8 dB @ 4 GHz of trace loss, followed by a Reference Receiver package, all behind a mated SFF-8639 connector interface. Assuming an 85-ohm differential trace structure with a loss of 0.8 dB @ 4 GHz per inch, the implied trace length is 18.5 inches and comprises 88% of the total system and module trace loss budget. This channel shall be referenced as the 8.0 GT/s SFF-8639 Module Test Channel. The s-parameters for the channel are provided with the specification. Note that additional loss from the measurement set-up shall be removed. Note that the 8.0 GT/s SFF-8639 Module Test Channel is a reference channel for testing and does not represent the worst possible channel that may be implemented in a compliant system.

961

4.6.4. SFF-8639 Module Minimum Receiver Path Sensitivity Requirements at 2.5 GT/s

The minimum sensitivity values for the SFF-8639 module's Receiver path compliance at 2.5 GT/s are defined in Table 4-12, and a representative eye diagram is shown in Figure 4-7.

Table 4-12. SFF-8639 Module Minimum Receiver Path Sensitivity Requirements at 2.5 GT/s

Parameter	Min	Max	Unit	Notes
V_{RXA}	238	1200	mV	Notes 1, 2, 5
V_{RXA_d}	219	1200	mV	Notes 1, 2, 5
T_{RXA}	246		ps	Notes 1, 3, 5
$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	77		ps	Notes 1, 4, 5

Notes:

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{RXA_d}). V_{RXA} and V_{RXA_d} are differential peak-peak output voltages.
3. T_{RXA} is the eye width. The sample size for this measurement is 10^6 UI. This value is able to be reduced to 233 ps for simulation purposes at BER 10^{-12}.
4. $T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum median-to-peak jitter outlier as defined in the latest *PCI Express Base Specification*. The sample size for this measurement is 10^6 UI. This value is able to be increased to 83.5 ps for simulation purposes at BER 10^{-612}.
5. The values in this table are initially referenced to an ideal 100 Ω differential load. The resultant values, when provided to the Receiver interconnect path of the SFF-8639 module, allow for a demonstration of compliance of the overall SFF-8639 module Receiver path. The sensitivity requirements are defined and centered with respect to the jitter median. Exact conditions required for verifying compliance against these values are given in the *PCI Express Architecture PHY Test Specification* document.

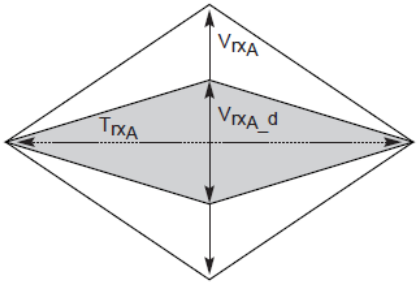


Figure 4-7. Representative Composite Eye Diagram for SFF-8639 Module Receiver Path Compliance

4.6.5. SFF-8639 Module Minimum Receiver Path Sensitivity Requirements at 5.0 GT/s

The minimum sensitivity values for the SFF-8639 module's Receiver path compliance at 5.0 GT/s are defined in Table 4-13, and a representative eye diagram is shown in Figure 4-7.

Table 4-13. SFF-8639 Module Minimum Receiver Path Sensitivity Requirements at 5.0 GT/s

Parameter	Min	Max	Unit	Notes
V_{RXA} V_{RXA_d}	225 225	1200 1200	mV mV	1, 2, 3 1, 2, 3
1.5 MHz – 100 MHz RMS Jitter	3.4		ps RMS	
33 kHz REFCLK Residual	75		ps PP	
< 1.5 MHz RMS Jitter	4.2		ps RMS	
1.5 MHz – 100 MHz Dj	30		ps PP	
> 100 MHz Dj	27		ps PP	

Notes:

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. This test requires transmission of the Compliance Pattern in 8b/10b Encoding, as defined in the *PCI Express Base Specification*.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{RXA_d}). V_{RXA} and V_{RXA_d} are differential peak-peak output voltages.
3. The values in this table are initially calibrated with a reference channel consisting of a 5.0 GT/s SFF-8639 Module Test Channel followed by a 5.0 GT/s SFF-8639 System Test Channel. After reference calibration, the 5.0 GT/s System Test Channel is removed and the SFF-8639 module to be tested is placed into the SFF-8639 bay connector. The resultant values, when provided to the Receiver interconnect path of the SFF-8639 module, allow for a demonstration of compliance of the overall SFF-8639 module Receiver path. The exact setup and methodology for injecting this signal into the Receiver interconnect path of the SFF-8639 module are not specified. The values in this table may need to be adjusted based on the exact test setup and methodology. For example, if the impedance of the test setup does not create the worst-case mismatch that may be present with a real system board or the test setup does not provide crosstalk (only a single Lane is tested, etc.) the values in this table must be adjusted accordingly.

4.6.6. SFF-8639 Module Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

The minimum sensitivity values for the SFF-8639 module's Receiver path compliance at 8.0 GT/s are defined in Table 4-14, Table 4-15, and Figure 4-7. The Receiver path must be tested with a worst-case eye to verify that it achieves a BER < 10^{-12}. This worst-case eye is calibrated using Transmitter equalization settings that are optimal with the reference equalizer for each calibration channel. After calibration, the test-generator's Transmitter equalization may be adjusted using the Transmitter equalization setting in the required Transmitter equalization space preferred by the module under test, without changing any other parameter of the test signal or recalibrating the test signal.

Note: If the test generator's Transmitter equalization settings are adjusted away from the optimal settings and the test generator is not able to change Transmitter equalization without impacting other calibrated parameters—then the other parameters must be adjusted back to the specified values.

If the test is not run in a way that produces the worst-case cross-talk present with all lanes active—the additional cross-talk must be accounted for in some other way.

The test is performed with two different test channels: a long test channel and a short test channel.

While the capacity of the Receiver to adapt to its own equalization is part of the test described above, its ability to request the Link Partner's Transmitter to change its Transmitter equalization is tested by applying a signal whose equalization level is suboptimal, compared to the jitter sensitivity test signal described above. For this signal, the Reference Receiver is not able to achieve proper equalization by means of its own continuous time linear equalizer (CTLE) and decision feedback equalizer (DFE) alone. Such a signal is defined using the signal resulting from the calibration method described above, and adjusting the test-generator equalization. Note that if the Receiver under test is more capable than the Reference Receiver (CTLE+DFE), the Receiver under test may not require the Transmitter to change its equalization levels to achieve a BER < 10^{-12}. In any case, equalization settings resulting from this procedure must be used for the above Receiver test. If the Receiver requires the Transmitter equalization to change, the change must be accommodated in the test set-up.

A specific methodology for this procedure is outside the scope of this specification. Refer to compliance program test procedures for specific test equipment for specific methodology details.

Table 4-14. Long Channel SFF-8639 Module Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

Parameter	Min	Max	Unit	Notes
$V_{RX-EH-8G}$ Eye Height	34	34	mV	1, 2, 4
$T_{RX-EW-8G}$ Eye Width	0.33	0.38	UI	1, 2, 5
Rj	3		ps RMS	5, 6
Sinusoidal Jitter (Sj) 100 MHz	12.5		ps PP	6
Differential Mode Sinusoidal Interference 2.1 GHz	14		mV PP	3

Notes:

1. An ideal reference clock without jitter is assumed for this specification. Calibration for this test is performed using the Compliance Pattern in 128b/130b Encoding (as defined in the *PCI Express Base Specification*). After calibration is complete, use the Modified Compliance Pattern in 128b/130b Encoding (as defined in the *PCI Express Base Specification*) for this test. Eye height and eye width values reference BER = 10^{-12}.
2. The values in this table are initially calibrated with a reference channel consisting of an 8.0 GT/s SFF-8639 Module Test Channel followed by an 8.0 GT/s SFF-8639 System Test Channel at the Transmitter connectors on the SFF-8639 System Test Channel. The calibration is done with the same post processing as the SFF-8639 System 8.0 GT/s Transmitter test. After reference calibration, the 8.0 GT/s SFF-8639 System Test Channel is removed and the SFF-8639 module to be tested is placed into an SFF-8639 bay connector.
3. Eye height and eye width are specified after the application of the Reference Receiver. When the optimization of the Reference Receiver CTLE and DFE yields an eye height and/or eye width larger than specified, the value for Differential Mode Sinusoidal Interference is increased.
4. Eye height limits do not account for limitations in test equipment voltage resolution.
5. The Rj bandwidth must be limited. The low frequency limit may be between 1.5 MHz and 10 MHz, and the upper limit is 1.0 GHz. While the minimum Rj magnitude is specified at 3.0 ps RMS, it may be adjusted to obtain the desired $T_{RX-EW-8G}$ Eye Width.
6. Rj and Sj are measured without post-processing filters.

1010 **Table 4-15. Short Channel SFF-8639 Module Minimum Receiver Path**
1011 **Sensitivity Requirements at 8.0 GT/s**

Parameter	Min	Max	Unit	Notes
$V_{RX-EH-8G}$ Eye Height	N/A	N/A	mV	1, 2, 5
$T_{RX-EW-8G}$ Eye Width	N/A	N/A	UI	1, 2, 5
Rj	3		ps RMS	4
Sj 100 MHz	12.5		ps PP	
Differential Mode Sinusoidal Interference 2.1 GHz.	14		mV PP	3

Notes:

1. An ideal reference clock without jitter is assumed for this specification. Calibration for this test is performed using the Compliance Pattern in 128b/130b Encoding (as defined in the *PCI Express Base Specification*). After calibration is complete, use the Modified Compliance Pattern in 128b/130b Encoding (as defined in the *PCI Express Base Specification*) for this test. Eye height and eye width values are in reference to a BER = 10^{-12}.
2. The values in this table are initially calibrated with a reference channel consisting of a 5.0 GT/s SFF-8639 Module Test Channel followed by a 5.0 GT/s SFF-8639 System Test Channel at the Transmitter connectors on the SFF-8639 System Test Channel. The calibration is done with the same post processing as the SFF-8639 System 5.0 GT/s Transmitter test. After reference calibration, the 5.0 GT/s SFF-8639 System Test Channel is removed and the SFF-8639 module to be tested is placed into an SFF-8639 bay connector.
3. Eye height and eye width are specified after application of the Reference Receiver. When Reference Receiver optimization yields an eye height and/or eye width larger than specified, the value for Differential Mode Sinusoidal Interference is increased.
4. The Rj bandwidth must be limited. The low frequency limit may be between 1.5 MHz and 10 MHz, and the upper limit is 1.0 GHz.
5. For the short channel test, the calibrated test equipment transmitter settings from the long channel test are used. Eye height and eye width are not separately re-calibrated.

1012

4.6.7. SFF-8639 System Transmitter Path Compliance Eye Diagram at 2.5 GT/s

The eye diagram for the SFF-8639 system's Transmitter compliance at 2.5 GT/s is defined in Table 4-16 and Figure 4-8.

Table 4-16. SFF-8639 System Transmitter Path Compliance Eye Requirements at 2.5 GT/s

Parameter	Min	Max	Unit	Notes
V_{TXS}	274	1200	mV	1, 2, 5
V_{TXS_d}	253	1200	mV	1, 2, 5
T_{TXS}	246		ps	1, 3, 5
$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$		77	ps	1, 4, 5

Notes:

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.
3. T_{TXS} is the minimum eye width. The sample size for this measurement is 10^6 UI. This value is able to be reduced to 233 ps for simulation purposes at BER 10^{-12}.
4. $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum median-to-max jitter outlier as defined in the *PCI Express Base Specification*. The sample size for this measurement is 10^6 UI. This value is able to be increased to 83.5 ps for simulation purposes at BER 10^{-12}.
5. The values in this table are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the SFF-8639 footprint on the SFF-8639 module when mated with the SFF-8639 bay connector (see Figure 4-5). The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PCI Express Architecture PHY Test Specification* document.

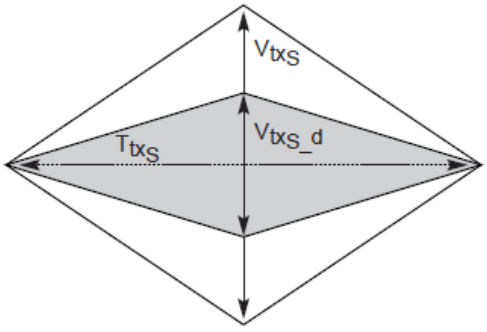


Figure 4-8. SFF-8639 System Transmitter Path Composite Compliance Eye Diagram

4.6.8. SFF-8639 System Transmitter Path Compliance Eye Diagram at 5.0 GT/s

The SFF-8639 system Transmitter path measurements at 5.0 GT/s are made using a two-port measurement methodology. Figure 4-9 shows a functional block diagram for an SFF-8639 system and SFF-8639 module that shows the measurement points for the two-port method.

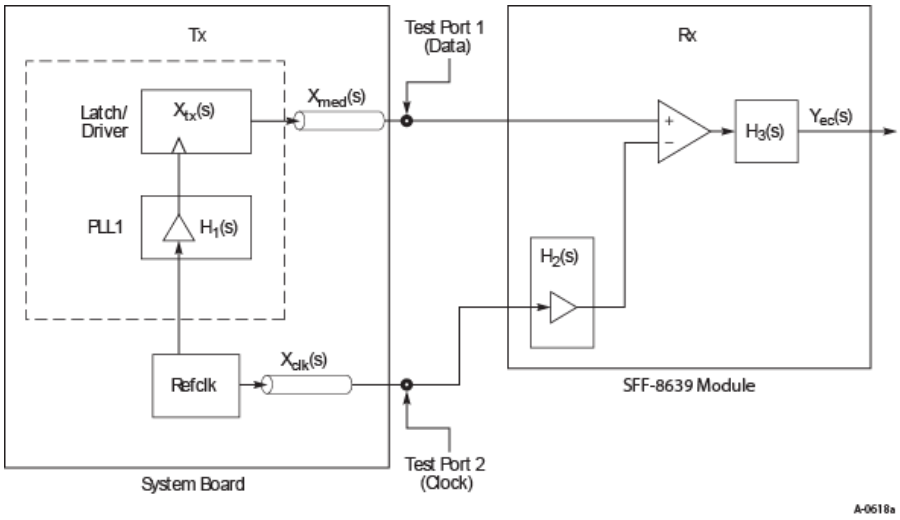


Figure 4-9. Two Port Measurement Functional Block Diagram

Equations for the jitter at Test Port 1 (Data) and Test Port 2 (Clock) and the eye closure at the SFF-8639 module Receiver from the test port signals are provided as follows:

- **Data Port Measurement (Test Port 1):**

$$\text{Eq.(1)} \qquad X_{dm}(s) = X_{clk}(s)H_1(s)e^{-sT_{d1a}} + X_{tx}(s) + X_{med}(s)$$

- **Clock Port Measurement (Test Port 2):**

$$\text{Eq.(2)} \qquad X_{cm}(s) = X_{clk}(s)e^{-sT_{d1b}}$$

- **Eye Closure at Receiver Due to Signals at Clock and Data Ports:**

$$\text{Eq.(3)} \quad Y_{ec}(s) = \{[X_{clk}(s)H_1(s)e^{-sT_{d1a}} + X_{tx}(s) + X_{med}(s)] - [X_{clk}(s)e^{-sT_{d1b}}][H_2(s)e^{-sT_{d2}}]\} \bullet H_3(s)$$

$$= (X_{dm}(s) - X_{clk}(s)H_2(s)e^{-sT_{d2}}) \bullet H_3(s)$$

where:

$X_{clk}(s)$ is the reference clock transfer function.
T_{d1a} is the delay from the reference clock to the data port.
T_{d1b} is the delay from the reference clock to the test port.
$X_{tx}(s)$ is the driver/latch transfer function.
$X_{med}(s)$ is the interconnect transfer function.
T_{d2} is the maximum reference clock transport delay introduced by the SFF-8639 module.
$H_1(s)$ is the Transmitter PLL transfer function as defined in the *PCI Express Base Specification.*
$H_2(s)$ is the Receiver PLL transfer function as defined in the *PCI Express Base Specification.*
$H_3(s)$ is the Phase Interpolator (PI) transfer function as defined in the *PCI Express Base Specification.*

The two-port measurement methodology and eye closure calculation are performed per the following steps:

- Data is gathered from Test Port 1 (Data) and Test Port 2 (Clock) to obtain the spectrum $X_{dm}(s)$ and $X_{cm}(s)$ or equivalent.
- The eye closure Yec(s) is calculated based on Eq (3). To obtain the maximum eye closure, sweep Td2 from -3 ns to +3 ns. H1(s) and H2(s) are defined below using the appropriate damping factor ζ and PLL bandwidth for each. H3(s) is defined in the *PCI Express Base Specification*:

$$H_1(s) = \frac{2s\zeta_1\omega_{n1+}\omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1} + \omega_{n1}^2} \qquad H_2(s) = \frac{2s\zeta_2\omega_{n2+}\omega_{n2}^2}{s^2 + 2s\zeta_2\omega_{n2} + \omega_{n2}^2} \qquad H_3(s) = \frac{s}{s + \omega_3}$$

where: $\zeta = 0.54$(3 *dB PK*), $\omega_{n2} = 8.61*2\pi$(16 *MHz 3dB BW) Mrad/s,* or
$\zeta = 0.54$(3 *dB PK*), $\omega_{n2} = 4.31*2\pi$(8 *MHz 3dB BW) Mrad/s,* or
$\zeta = 1{,}16$(1 *dB PK*), $\omega_{n2} = 1.82*2\pi$(5 *MHz 3dB BW) Mrad/s*

- Calculate the eye closure at BER = 10^{-12} from $Y_{ec}(t)$, the inverse Fast Fourier Transform of $Y_{ec}(s)$. The maximum eye closure for any parameters of T_{d2} and $H_2(s)$ in the defined ranges is the total jitter assigned to the system board Transmitter + Transmitter interconnect + reference clock.

The SFF-8639 system Transmitter path compliance eye requirements at 5.0 GT/s are given in Table 4-17 and Figure 4-8 shows the eye diagram.

Table 4-17. SFF-8639 System Transmitter Path Compliance Eye Requirements at 5.0 GT/s

Parameter	Min	Max	Unit	Notes
V_{TXS}	190	1200	mV	1, 2, 4
V_{TXS_d}	190	1200	mV	1, 2, 4
T_{TXS} (with crosstalk)	95		ps	1, 3, 4
T_{TXS} (without crosstalk)	108		ps	

Notes:

1. All Links are assumed active while generating this eye diagram. The eye diagram requires transmission of the Compliance Pattern in 8b/10b Encoding (*PCI Express Base Specification*) during the test using the de-emphasis level that the SFF-8639 system will use in normal operation.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.
3. T_{TXS} is the minimum eye width. The recommended sample size for the two-port measurement is at least 10^6 UI. The minimum eye opening at BER 10^{-12} is calculated based on the measured data and must not exceed T_{TXS}.
4. The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated 2 inch 85 Ω differential trace behind the mated SFF-8639 module connector interface. This channel must be referenced as the 5.0 GT/s SFF-8639 System Test Channel. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PCI Express Architecture PHY Test Specification* document.

The SFF-8639 system total jitter for the Transmitter + Transmitter interconnect + reference clock must meet the requirements listed in Table 4-18 when decomposed into random and deterministic jitter.

Table 4-18. SFF-8639 System Jitter Requirements for 5.0 GT/s Signaling

	Max Rj (ps RMS)	Max Dj (ps)	Tj at BER 10^{-12} (ps)
With crosstalk	3.41	57	105
Without crosstalk	3.41	44	92

4.6.9. SFF-8639 System Transmitter Path Compliance Eye Diagram at 8.0 GT/s

The SFF-8639 system must pass the eye diagram requirements with at least one of the Transmitter equalization presets defined in the *PCI Express Base Specification*. The eye diagram requirements are evaluated after the behavioral CDR defined in the *PCI Express Base Specification* and the behavioral Receiver Equalization Algorithm defined in the *PCI Express Base Specification*.

The SFF-8639 system Transmitter path measurements at 8.0 GT/s are made using a two-port measurement methodology. Figure 4-10 shows the functional block diagram for an SFF-8639 system and SFF-8639 module that shows the measurement points for the two-port method.

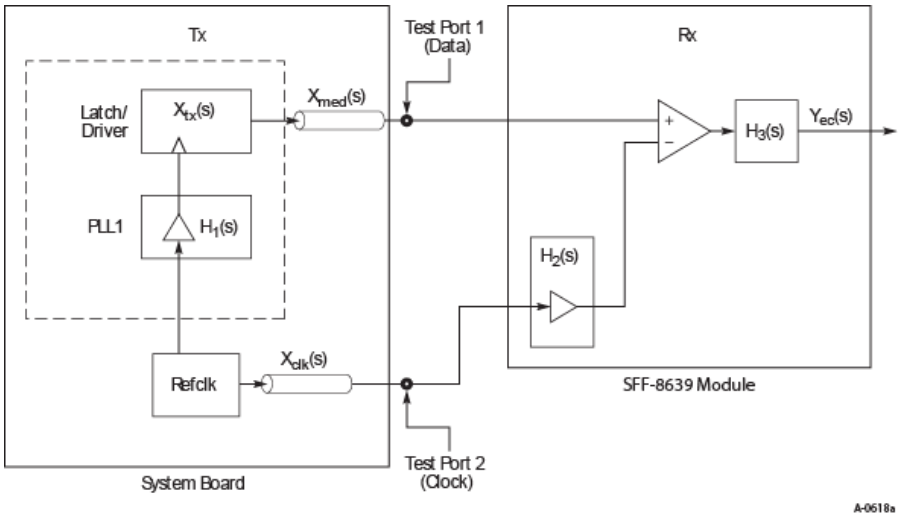


Figure 4-10. Two port Measurement Functional Block Diagram

Equations for the jitter at Test Port 1 (Data), Test Port 2 (Clock), and the eye closure at the SFF-8639 Receiver from the test port signals are provided as follows:

- **Data Port Measurement (Test Port 1)**

Eq.(1) $$X_{dm}(s) = X_{clk}(s)H_1(s)e^{-sT_{d1a}} + X_{tx}(s) + X_{med}(s)$$

- **Clock Port Measurement (Test Port 2)**

Eq.(2) $$X_{cm}(s) = X_{clk}(s)e^{-sT_{d1b}}$$

- **Eye Closure at Receiver Due to Signals at Clock and Data Ports**

Eq.(3) $$Y_{ec}(s) = \{[X_{clk}(s)H_1(s)e^{-sT_{d1a}} + X_{tx}(s) + X_{med}(s)] - [X_{clk}(s)e^{-sT_{d1b}}][H_2(s)e^{-sT_{d2}}]\} \bullet H_3(s)$$

$$= (X_{dm}(s) - X_{clk}(s)H_2(s)e^{-sT_{d2}}) \bullet H_3(s)$$

where:

$X_{clk}(s)$ is the reference clock transfer function

T_{d1a} is the delay from the reference clock to the data port

T_{d1b} is the delay from the reference clock to the test port

$X_{tx}(s)$ is the driver/latch transfer function

$X_{med}(s)$ is the interconnect transfer function

T_{d2} is the maximum reference clock transport delay introduced by the SFF-8639 module

$H_1(s)$ is the Transmitter PLL transfer function as defined in the *PCI Express Base Specification*

$H_2(s)$ is the Receiver PLL transfer function as defined in the *PCI Express Base Specification*

$H_3(s)$ is the Phase Interpolator (PI) transfer function as defined in the *PCI Express Base Specification*

The two-port measurement methodology and eye closure calculation are performed using the following steps:

- Data is gathered from Test Port 1 (Data) and Test Port 2 (Clock) to obtain the spectrum $X_{dm}(s)$ and $X_{cm}(s)$ or equivalent.
- The eye closure $Y_{ec}(s)$ is calculated based on Eq (3). To obtain the maximum eye closure, sweep T_{d2} from -3 ns to +3 ns. $H_1(s)$ and $H_2(s)$ are defined below using the appropriate damping factor ζ and PLL bandwidth for each. $H_3(s)$ is defined in the *PCI Express Base Specification*:

$$H_1(s) = \frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + 2s\zeta_1\omega_{n1} + \omega_{n1}^2} \qquad H_2(s) = \frac{2s\zeta_2\omega_{n2} + \omega_{n2}^2}{s^2 + 2s\zeta_2\omega_{n2} + \omega_{n2}^2} \qquad H_3(s) = \frac{s}{s + \omega_3}$$

where: $\zeta = 0.73$(2 *dB PK*), $\omega_{n2} = 6.1$(2 *MHz 3dB BW) Mrad/s,* or
$\zeta = 0.73$(2 *dB PK*), $\omega_{n2} = 12.2$(4 *MHz 3dB BW) Mrad/s,* or
$\zeta = 1.15$(1 *dB PK*), $\omega_{n2} = 11.53$ (5 *MHz 3dB BW) Mrad/s*

- Calculate the eye closure at BER = 10^{-12} from $Y_{ec}(t)$, the inverse Fast Fourier Transform of $Y_{ec}(s)$. The maximum eye closure for any parameters of T_{d2} and $H_2(s)$ in the defined ranges is the total jitter assigned to the system board Transmitter + Transmitter interconnect + reference clock.

The SFF-8639 system Transmitter path compliance eye requirements at 8.0 GT/s are given in Table 4-19 and Figure 4-8 shows the eye diagram.

Table 4-19. SFF-8639 System Transmitter Path Compliance Eye Requirements at 8.0 GT/s with Ideal Adaptive Transmitter Equalization

Parameter	Min	Max	Unit	Notes
V_{TXS}	34	1200	mV	1, 2, 4
V_{TXS_d}	34	1200		1, 2, 4
T_{TXS}	41.25		ps	1, 3, 4

Notes:

1. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (*PCI Express Base Specification)* is being transmitted during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. For lab use, an informative voltage limit (V_{TXS} and V_{TXS_d}) at a BER of 10^{-6} is 46 mV.
3. T_{TXS} is the minimum eye width. The recommended sample size for this measurement is at least 10^6 UI. The calculated eye width at BER = 10^{-12} must not exceed T_{TXS}.
4. The values in this table are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel, consisting of 2 dB @ 4 GHz of trace loss, followed by a Reference Receiver package, all behind a mated SFF-8639 connector interface. Assuming an 85-ohm differential trace structure with a loss of 0.8 dB @ 4 GHz per inch, the implied trace length is 2.5 inches and comprises 12% of the total system and module trace loss budget. This channel shall be referenced as the 8.0 GT/s SFF-8639 System Test Channel. The s-parameters for the channel are provided with the specification. Note that additional loss from the measurement set-up shall be removed. Note that the 8.0 GT/s SFF-8639 System Test Channel is a reference channel for testing and does not represent the worst possible channel that may be implemented in a compliant system.

4.6.10. SFF-8639 System Minimum Receiver Path Sensitivity Requirements at 2.5 GT/s

The minimum sensitivity values for the SFF-8639 system's Receiver path compliance at 2.5 GT/s are defined in Table 4-20. A representative eye diagram is shown in Figure 4-11.

Table 4-20. SFF-8639 System Minimum Receiver Path Sensitivity Requirements at 2.5 GT/s

Parameter	Min	Max	Unit	Notes
V_{RXS}	445	1200	mV	1, 2, 5
V_{RXS_d}	312	1200	mV	1, 2, 5
T_{RXS}	287		ps	1, 3, 5
$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	56.5		ps	1, 4, 5

Notes:

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires transmission of the Compliance Pattern in 8b/10b Encoding (*PCI Express Base Specification*) during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{RXS_d}). V_{RXS} and V_{RXS_d} are differential peak-peak output voltages.
3. T_{RXS} is the eye width. The sample size for this measurement is 10^6 UI. This value is able to be reduced to 274 ps for simulation purposes at BER 10^{-12}.
4. $T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum median-to-peak jitter outlier as defined in the *PCI Express Base Specification*. The sample size for this measurement is 10^6 UI. This value is able to be increased to 63 ps for simulation purposes at BER 10^{-12}.
5. The values in this table are referenced to an ideal 100 Ω differential load at the end of 85 Ω differential isolated 3 inch traces behind the mated SFF-8639 connector interface. The resultant values, when provided to the Receiver interconnect path of the SFF-8639 system, allow for a demonstration of compliance of the overall SFF-8639 system Receiver path. The sensitivity requirements are defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PCI Express Architecture PHY Test Specification* document.

4.6.11. SFF-8639 System Minimum Receiver Path Sensitivity Requirements at 5.0 GT/s

The minimum sensitivity values for the SFF-8639 system's Receiver path compliance at 5.0 GT/s are defined in Table 4-21 and Table 4-22. A representative eye diagram is shown in Figure 4-11.

Table 4-21. SFF-8639 System Minimum Receiver Path Sensitivity Requirements at 5.0 GT/s for a Link that Operates with 3.5 dB De-emphasis

Parameter	Min	Max	Unit	Notes
V_{RXS}	380	1200	mV	1, 2, 3
V_{RXS_d}	380	1200	mV	1, 2, 3
1.5 – 100 MHz RMS Jitter	1.4		ps RMS	
< 1.5 MHz RMS Jitter	3.0		ps RMS	
1.5 – 100 MHz Dj	30		ps PP	
> 100 MHz Dj	27		ps PP	

Notes:

1. All Links are assumed active while generating this eye diagram. The eye diagram requires transmission of the Compliance Pattern in 8b/10b Encoding (*PCI Express Base Specification*) during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{RXS_d}). V_{RXS} and V_{RXS_d} are differential peak-peak output voltages.
3. The values in this table are calibrated with a reference channel consisting of a 5.0 GT/s SFF-8639 System Test Channel followed by a 5.0 GT/s SFF-8639 Module Test Channel. After reference calibration, the 5.0 GT/s SFF-8639 Module Test Channel is removed, and an SFF-8639 module is placed into the SFF-8639 module bay to be tested. The resultant values, when provided to the Receiver interconnect path of the system board, allow for a demonstration of compliance of the overall SFF-8639 system Receiver path. The exact setup and methodology for injecting this signal into the Receiver interconnect path of the SFF-8639 system are not specified. The values in this table may need to be adjusted based on the exact test setup and methodology. For example, if the impedance of the test setup does not create the worst-case mismatch that may be present with a real SFF-8639 module or the test setup does not provide crosstalk (only a single Lane is tested, etc.), the values in this table must be adjusted accordingly.

Table 4-22. SFF-8639 System Minimum Receiver Path Sensitivity Requirements at 5.0 GT/s for a Link that Operates with 6.0 dB De-emphasis

Parameter	Min	Max	Unit	Notes
V_{RXS}	306	1200	mV	1, 2, 3
V_{RXS_d}	260	1200	mV	1, 2, 3
1.5 MHz – 100 MHz RMS Jitter	1.4		ps RMS	
< 1.5 MHz RMS Jitter	3.0		ps RMS	
1.5 MHz – 100 MHz Dj	30		ps PP	
> 100 MHz Dj	27		ps PP	

Notes:

1. All Links are assumed active while generating this eye diagram. The eye diagram requires transmission of the Compliance Pattern in 8b/10b Encoding (*PCI Express Base Specification*) during the test.
2. Transition and non-transition bits must be distinguished to measure compliance against the de-emphasized voltage level (V_{RXS_d}). V_{RXS} and V_{RXS_d} are differential peak-peak output voltages.
3. The values in this table are referenced to an ideal 100 Ω differential load behind a 3-inch isolated 85 Ω trace and a mated SFF-8639 connector interface. After reference calibration, the reference fixture is removed, and an SFF-8639 module is placed into the SFF-8639 bay to be tested. The resultant values, when provided to the Receiver interconnect path of the SFF-8639 system, allow for a demonstration of compliance of the overall SFF-8639 system Receiver path. The exact setup and methodology for injecting this signal into the Receiver interconnect path of the SFF-8639 system are not specified. The values in this table may need to be adjusted based on the exact test setup and methodology. For example, if the impedance of the test setup does not create the worst-case mismatch that may be present with a real SFF-8639 module or the test setup does not provide crosstalk (only a single Lane is tested, etc.) the values in this table must be adjusted accordingly.

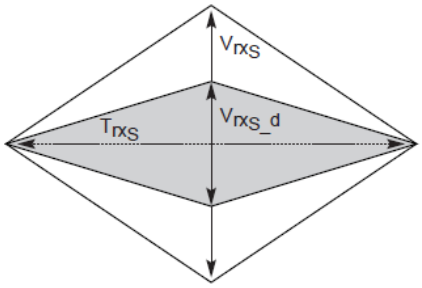


Figure 4-11. Representative Composite Eye Diagram for SFF-8639 System Receiver Path Compliance

4.6.12. SFF-8639 System Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

The minimum sensitivity values for the SFF-8639 system Receiver path compliance at 8.0 GT/s are defined in Table 4-23. The corresponding eye diagram is illustrated in Figure 4-11. The Receiver path must be tested with a worst-case eye to verify that it achieves a BER < 10^{-12}. This worst-case eye is calibrated using Transmitter equalization settings that are optimal with the reference equalizer for the calibration channel. After calibration, the test-generator's equalization settings may be adjusted using the Transmitter equalization setting in the required Transmitter equalization space preferred by the system under test, without changing any other parameter of the test signal or recalibrating the test signal.

Note: If the test generator's Transmitter equalization settings are adjusted away from the optimal settings and the test generator is not able to change Transmitter equalization without impacting other calibrated parameters—then the other parameters must be adjusted back to the specified values.

If the test is not run in a way that produces the worst-case cross-talk present with all lanes active, the additional cross-talk must be accounted for in some other way.

While the capacity of the Receiver to adapt its own equalization is part of the test described above, its ability to request the Link Partner's Transmitter to change its equalization settings is tested by applying a signal whose equalization settings are sub-optimal, compared to the jitter sensitivity test signal described above. For this signal, the Reference Receiver is not able to achieve proper equalization by means of its own CTLE and DFE, alone. Such a signal is defined using the signal resulting from the calibration method described above and adjusting the test-generator equalization. Note that if the Receiver under test is more capable than the Reference Receiver (CTLE+DFE), the Receiver may not require the Transmitter to change its equalization levels to achieve a BER < 10^{-12}. In any case, equalization settings resulting from this procedure must be used for the above Receiver test and, if the Receiver requires the Transmitter equalization to change, such change must be accommodated by the test set-up used.

A specific methodology for this procedure is outside the scope of this specification.

Table 4-23. SFF-8639 System Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

Parameter	Min	Max	Unit	Notes
$V_{RX-EH-8G}$ Eye height	34	34	mV	1, 2, 4
$T_{RX-EW-8G}$ Eye width	0.33	0.38	UI	1, 2
Rj	3		ps RMS	5, 6
Sj 100 MHz	12.5		ps PP	6
Differential Mode Sinusoidal Interference 2.1 GHz	14		mV PP	3

Notes:

1. The system board reference clock is assumed for this specification. Calibration for this test is performed using the Compliance Pattern in 128b/130b Encoding (as defined in the *PCI Express Base Specification*). After calibration is complete, use the Modified Compliance Pattern in 128b/130b Encoding (as defined in the *PCI Express Base Specification*) for this test. Eye height and eye width values reference BER = 10^{-12}.
2. The values in this table are initially calibrated with a reference channel consisting of an 8.0 GT/s SFF-8639 System Test Channel followed by an 8.0 GT/s SFF-8639 Module Test Channel at the Transmitter connectors on the SFF-8639 Module Test Channel. The calibration is done with the same post processing as the SFF-8639 8.0 GT/s Transmitter test. After reference calibration, the 8.0 GT/s SFF-8639 Module Test Channel is removed, and the SFF-8639 System Test Channel is connected to the SFF-8639 System to be tested.
3. Eye height and eye width are specified after the application of the Reference Receiver. When Reference Receiver optimization yields an eye height and/or eye width larger than specified, the value for Differential Mode Sinusoidal Interference is increased.
4. Eye height limits do not account for limitations in test equipment voltage resolution.
5. The Rj bandwidth must be limited. The low frequency limit may be between 1.5 MHz and 10 MHz, and the upper limit is 1.0 GHz. While the ~~nominal~~ minimum value is specified at 3.0 ps RMS, it may be adjusted to meet the value for $T_{RX-EW-8G}$ Eye Width.

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1185 5. SFF-8639 Connector Specification

1186 Contact functionality is documented in *SFF-9639: Multifunction 6X Unshielded Connector Pinouts*.
1187 Mechanical details are documented in *SFF-8639: Multifunction 6X Unshielded Connector*. Information
1188 provided in this chapter is supplemental and applies only to the PCI-Express implementation of
1189 SFF-8639.

1190 5.1. Connector Pinout

1191 Table 5-1 shows the pinout definition, including the mating sequence (Mate) and the signal type
1192 (Type), with respect to the system side of the interface and not the module. Signals described as
1193 outside the scope of this specification apply to legacy storage interfaces.

1194 **Table 5-1. SFF-8639 PCI Express Connector Pinout**

Pin	Mate	Name	Type	Description
P1	3rd	WAKE#	Bi-Dir	Signal for Link reactivation
P2	3rd	-	-	Outside scope of this specification (See SFF-8639)
P3	2nd	PWRDIS	Output	Power disable
P4	1st	IfDet#	Input	Interface Type Detect
P5	2nd	Ground	Ground	Ground
P6	2nd	Ground	Ground	Ground
P7	2nd	-	-	Outside scope of this specification (See SFF-8639)
P8	3rd	-	-	Outside scope of this specification (See SFF-8639)
P9	3rd	-	-	Outside scope of this specification (See SFF-8639)
P10	2nd	PRSNT#	Input	Presence detect
P11	3rd	ACTIVITY#	Input	Activity indicator
P12	1st	Ground	Ground	Ground
P13	2nd	+12 V Precharge	Power	+12 V Precharge power for SFF-8639 module

Pin	Mate	Name	Type	Description
P14	3rd	+12 V	Power	+12 V power for SFF-8639 module
P15	3rd	+12 V	Power	+12 V power for SFF-8639 module
S1	2nd	Ground	Ground	Ground
S2	3rd	-	-	Outside scope of this specification (See SFF-8639)
S3	3rd	-	-	Outside scope of this specification (See SFF-8639)
S4	2nd	Ground	Ground	Ground
S5	3rd	-	-	Outside scope of this specification (See SFF-8639)
S6	3rd	-	-	Outside scope of this specification (See SFF-8639)
S7	2nd	Ground	Ground	Ground
S8	2nd	Ground	Ground	Ground
S9	3rd	-	-	Outside scope of this specification (See SFF-8639)
S10	3rd	-	-	Outside scope of this specification (See SFF-8639)
S11	2nd	Ground	Ground	Ground
S12	3rd	-	-	Outside scope of this specification (See SFF-8639)
S13	3rd	-	-	Outside scope of this specification (See SFF-8639)
S14	2nd	Ground	Ground	Ground
S15	3rd	Reserved	-	Reserved
S16	2nd	Ground	Ground	Ground
S17	3rd	PETp1	Diff-Pair	Transmitter differential pair, Lane 1
S18	3rd	PETn1	Diff-Pair	Transmitter differential pair, Lane 1
S19	2nd	Ground	Ground	Ground
S20	3rd	PERn1	Diff-Pair	Receiver differential pair, Lane 1
S21	3rd	PERp1	Diff-Pair	Receiver differential pair, Lane 1
S22	2nd	Ground	Ground	Ground
S23	3rd	PETp2	Diff-Pair	Transmitter differential pair, Lane 2
S24	3rd	PETn2	Diff-Pair	Transmitter differential pair, Lane 2
S25	2nd	Ground	Ground	Ground
S26	3rd	PERn2	Diff-Pair	Receiver differential pair, Lane 2
S27	3rd	PERp2	Diff-Pair	Receiver differential pair, Lane 2

Pin	Mate	Name	Type	Description
S28	2nd	Ground	Ground	Ground
E1	3rd	REFCLKB+	Diff-Pair	Reference clock for second x2 port
E2	3rd	REFCLKB-	Diff-Pair	Reference clock for second x2 port
E3	3rd	+3.3 Vaux	Power	+3.3 V auxiliary power
E4	3rd	CLKREQ#/PERSTB#	Bi-Dir	Clock request/Fundamental reset for second x2 port
E5	3rd	PERST#	Output	Fundamental reset (if Dual port mode enabled, first x2 port)
E6	3rd	Reserved	-	Reserved
E7	3rd	REFCLK+	Diff-Pair	Reference clock (if Dual port mode enabled, first x2 port)
E8	3rd	REFCLK-	Diff-Pair	Reference clock (if Dual port mode enabled, first x2 port)
E9	2nd	Ground	Ground	Ground
E10	3rd	PETp0	Diff-Pair	Transmitter differential pair, Lane 0
E11	3rd	PETn0	Diff-Pair	Transmitter differential pair, Lane 0
E12	2nd	Ground	Ground	Ground
E13	3rd	PERn0	Diff-Pair	Receiver differential pair, Lane 0
E14	3rd	PERp0	Diff-Pair	Receiver differential pair, Lane 0
E15	2nd	Ground	Ground	Ground
E16	3rd	Reserved	-	Reserved
E17	3rd	PETp3	Diff-Pair	Transmitter differential pair, Lane 3
E18	3rd	PETn3	Diff-Pair	Transmitter differential pair, Lane 3
E19	2nd	Ground	Ground	Ground
E20	3rd	PERn3	Diff-Pair	Receiver differential pair, Lane 3
E21	3rd	PERp3	Diff-Pair	Receiver differential pair, Lane 3
E22	2nd	Ground	Ground	Ground
E23	3rd	SMBCLK	Bi-Dir	SMBus (System Management Bus) clock
E24	3rd	SMBDAT	Bi-Dir	SMBus (System Management Bus) data
E25	3rd	DualPortEn#	Output	Dual port Enable

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Note the following points:

- The PCI Express interface pins PETpx, PETnx, PERpx, and PERnx are named with the following convention:
  - ***PE*** stands for PCI Express
  - ***T*** for *Transmitter*
  - ***R*** for *Receiver*
  - ***p*** for *positive* (+)
  - ***n*** for *negative* (-)
  - ***x*** for Lane number
- By default, PETpx and PETnx pins (the Transmitter differential pair of the connector) must be connected to the PCI Express Transmitter differential pair on the system board, and to the PCI Express Receiver differential pair on the SFF-8639 module.
- By default, PERpx and PERnx pins (the Receiver differential pair of the connector) must be connected to the PCI Express Receiver differential pair on the system board, and to the PCI Express Transmitter differential pair on the SFF-8639 module.
- However, the ***p*** and ***n*** connections may be reversed to simplify PCB trace routing and minimize vias if needed. All PCI-Express Receivers incorporate automatic Lane Polarity Inversion as part of the Link Initialization and Training and will correct the polarity independently on each Lane. Refer to the *PCI Express Base Specification*.
- If the SFF-8639 module does not support the optional PCI Express Lane Reversal functions, it must connect each Transmitter and Receiver Lane to the SFF-8639 connector lanes as shown in Table 5-1. For example, a x4 component must connect Lane 0 to 0, Lane 1 to 1, Lane 2 to 2, and Lane 3 to 3.
- Signals CLKREQ# and PERSTB# are assigned to the same physical pin. Optional signal PERSTB# is valid when the module is configured for Dual port mode. Optional signal CLKREQ# is valid only when the module is NOT configured for Dual port mode.
- If the component on the system board or SFF-8639 module supports the optional PCI Express Lane Reversal function, it may connect each Transmitter and Receiver Lane to the SFF-8639 module connector Lanes as shown in Table 5-1 or it may connect the Transmitter and Receiver Lanes using a reversed Lane ordering. Either Lane ordering may be used to simplify PCB trace routing and minimize vias. However, the transmitting and receiving Lanes must be connected with the same Lane ordering. For example, a x4 component may connect Lane 0 to 0, Lane 1 to 1, Lane 2 to 2, and Lane 3 to 3, or it may connect Lane 0 to 3, Lane 1 to 2, Lane 2 to 1, and Lane 3 to 0.

Note: Consistent with the *PCI Express Base Specification*, negotiation with SFF-8639 modules or systems implemented with fewer than four lanes (x1 or x2) must be supported.

- See Chapter 2 for Auxiliary signals description and implementation, except the +3.3 Vaux and PRSNT# and IfDet# pins. The requirements for +3.3 Vaux are discussed in Chapter 4. The PRSNT# and IfDet# signals are used for module presence detect and are discussed in Chapter 3.
- Power pins (+3.3 Vaux, and +12 V) are defined based on the PCI Express power delivery requirements specified in Chapter 4, *Electrical Requirements*, with the connector contact carrying capability being 1.5 A (continuous) per pin.

- The SFF-8639 module must be +3.3 V tolerant on pins P1, P2 and P3.
- The SFF-8639 bay must be tolerant of modules where pins P1, P2 and P3 are electrically connected. Note that such a connection is not supported by PCI Express.

5.2. Signal Integrity Requirements and Test Procedures

5.2.1. Signal Integrity Requirements

The procedures outlined in the following ANSI Electronics Industry Alliance (EIA) standards documents must be followed:

- EIA 364-101 – *Attenuation Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems*
- EIA 364-90 – *Crosstalk Ratio Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems*
- EIA 364-108 – *Impedance, Reflection Coefficient, Return Loss, and VSWR Measured in the Time and Frequency Domain Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems*

5.2.2. Signal Integrity Requirements and Test Procedures for 8.0 GT/s Support

An electrical test fixture must be used for evaluating connector signal integrity. The test fixture effects, not including the SFF-8639 connector footprint, must be de-embedded from all measurements. A section is provided with test fixture requirements and recommendations.

Table 5-2 lists the electrical signal integrity parameters, requirements, and test procedures.

1260 **Table 5-2. Signal Integrity Requirements and Test Procedures for**
1261 **8.0 GT/s Support**

Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard must be used with the following considerations: • The measured differential s-parameter must be referenced to 85 Ω differential impedance. • The test fixture must meet the test fixture requirement defined in Section 5.2.2.1. • The test fixture effect must be removed from the measured s-parameters. See Note 1.	≥ -0.5 dB up to 2.5 GHz; ≥ -[0.8*(f-2.5)+0.5] dB for 2.5 GHz < f ≤ 5 GHz (for example, ≥ -2.5 dB at f = 5 GHz) ≥ -[3.0*(f-5)+2.5] dB for 5 GHz < f ≤ 12 GHz (for example, ≥ -10 dB at f = 7.5 GHz)
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard must be used with the following considerations: • The measured differential s-parameter must be referenced to 85 Ω differential impedance. • The test fixture must meet the test fixture requirement in Section 5.2.2.1. • The test fixture effect must be removed. See Note 1.	≤ -15 dB up to 3.0 GHz; ≤ 5*f - 30 dB for 3.0 GHz < f ≤ 5 GHz; ≤ -1 dB for 5.0 GHz < f ≤ 12 GHz
Intra-pair Skew	Intra-pair skew must be achieved by design; measurement not required.	5 ps max
Differential Near End Crosstalk (DDNEXT)	EIA 364-90 The EIA standard must be used with the following considerations: • The crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector, as illustrated in Figure 5-1. • This is a differential crosstalk requirement between a victim differential signal pair and all of its adjacent differential signal pairs. The measured differential s-parameter must be referenced to 85 Ω differential impedance.	≤ -32 dB up to 2.5 GHz; ≤ -26 dB for 2.5 GHz < f ≤ 5.0 GHz; ≤ -20 dB for 5.0 GHz < f ≤ 10 GHz; < -10 dB for 10 GHz < f ≤ 12 GHz

Notes:

1. The specified s-parameters requirements are for connector only, not including the test fixture effect. Although the TRL calibration method is recommended, other calibration methods are allowed.

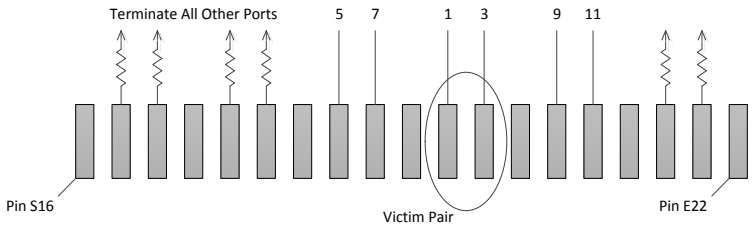

Figure 5-1. Illustration of Adjacent Pairs

5.2.2.1. Test Fixture Requirements

The test fixture for connector s-parameter measurements must be designed and built to the following requirements:

- The total thickness of the test fixture PCB must be 1.57 mm (0.062 inch) and both test fixtures must be a break-out card fabricated in the same PCB panel for the fixture.
- Traces between the connector and measurement ports (SMA or microprobe) must be uncoupled.
- The trace lengths between the connector and measurement port must be minimized. The maximum trace length must not exceed 45.72 mm (1.8 inch). The trace lengths between the connector and measurement port on the plug and receptacle fixtures must be equal.
- All the traces on the test board must be held to a characteristic impedance of 50 Ω with a tolerance of ±7 Ω.
- Use of SMA connectors is recommended. The SMA launch structure must be designed to minimize the connection discontinuity from SMA to the trace. The impedance range of the SMA seen from a TDR with a 30 ps rise time is recommended to be within 50 Ω with tolerance of ± 7 Ω.
- If a fixture with other characteristics is used, the fixture effects must be reliably removed and must not impact measurement accuracy.

5.3. Connector Environmental and Other Requirements

5.3.1. Environmental Requirements

Environmental requirements are defined in the *SFF-8639: Multifunction 12 Gb/s 6X Unshielded Connector* specification.

5.3.2. Mechanical Requirements

Mechanical requirements are defined in the *SFF-8639: Multifunction 12 Gb/s 6X Unshielded Connector* specification.

5.3.3. Current Rating Requirement

The current rating requirements are defined in the *SFF-8639: Multifunction 12 Gb/s 6X Unshielded Connector* specification.

6

6. SFF-8639 Module Form Factor

The SFF-8639 module shares the form factor of legacy storage devices that are already available in the industry.

6.1. Module Form Factor

The *SFF-8201: 2.5" Form Factor Drive Dimensions* specification provides detailed dimensioning of the industry standard 2.5-inch disk drive form factor. The location of the SFF-8639 connector is not provided.

6.2. Location of Connector on Module Form Factor

The *SFF-8223: 2.5" Form Factor Drive with Serial Attached Connector* specification provides detailed locational dimensioning of the SFF-8639 connector in the SFF-8201 form factor.

A

Appendix A. Insertion Loss Values

(Voltage Transfer Function) (Informational Only)

The maximum loss values in dB (decibels) are specified for the SFF-8639 system and the SFF-8639 module. The insertion loss values are defined as the ratio of the voltage at the ASIC package pin (Transmitter/Receiver) and the voltage at the PCI Express connector interface, terminated by 100 Ω differential termination, realized as two 50 Ω resistances. The instrumentation setup, including termination resistances, is illustrated in Figure A-1.

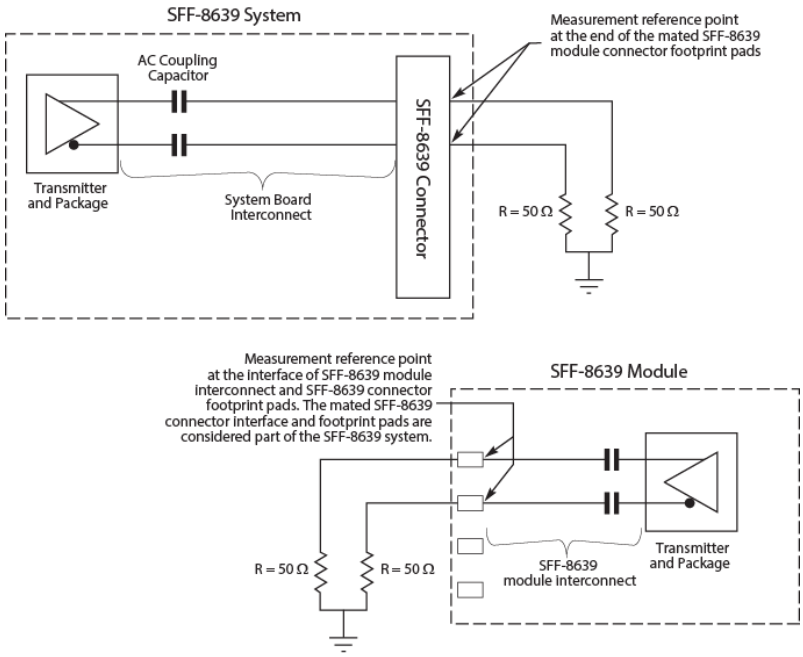

Figure A-1. Example of Interconnect Terminated at the Connector Interface

All PCI Express differential trace pairs are required to be referenced to the ground plane. The loss values associated with any cable and/or backplane riser card interface and adjoining connector implementation must collectively meet the system board loss budget allocations and associated eye diagrams.

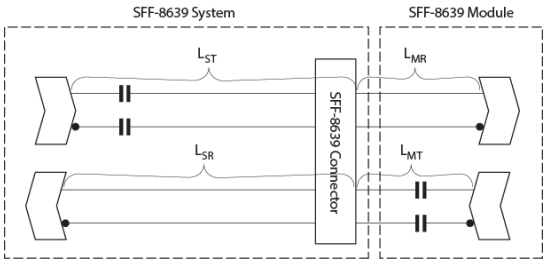

Figure A-2. Insertion Loss Budgets

Table A-1. Allocation of Interconnect Path Insertion Loss Budget for 2.5 GT/s Signaling

Loss Parameter	Loss Budget Value at 1.25 GHz (dB)		Loss Budget Value at 625 MGHz (dB)		Note
SFF-8639 Module	L_{MR} < 2.65	L_{MT} < 3.84	L_{MR} < 1.95	L_{MT} < 2.94	1, 2
SFF-8639 System (including interconnect and mated SFF-8639 connector interface)	L_{ST} < 9.30	L_{SR} < 8.11	L_{ST} < 6.00	L_{SR} < 5.01	1, 3
Guard Band	1.25	1.25			1
Total Loss	L_T < 13.2		L_T < 9.2		

Notes:

1. All values are referenced to 100 Ω, realized as two 50 Ω resistances. The loss budget values include all possible crosstalk impacts (near-end and far-end) and potential mismatch of the actual interconnect with respect to the 100 Ω reference load.
   The *PCI Express Base Specification* allows an interconnect loss of 13.2 dB for 1.25 GHz (no de-emphasis) signals and 9.2 dB for 625 MHz (de-emphasized) signals. From this, a total of 1.25 dB is held in reserve as guard band to allow for any additional attenuation that may occur when the SFF-8639 module and bay are mated. The allocated loss budget values in the table directly correlate to the eye diagram voltages in Section 4.6. Tradeoffs in terms of attenuation, crosstalk, and mismatch are made within the budget allocations specified.
   As a guide for design and simulation, the following derivation of the budgets may be assumed for 1.25 GHz signals: 5.2 dB is subtracted from 13.2 dB to account for near-end crosstalk and impedance mismatches. Out of this, 1.25 dB is reserved as guard band. The following loss allocations are then assumed per differential pair: L_{MR} = 1.4 dB; L_{MT} = 1.8 dB; L_{SR} = 6.2 dB; L_{ST} = 6.6 dB. These allocation assumptions must also include any effects of far-end crosstalk. 625 MHz values may be derived in a similar manner.
2. The SFF-8639 module budget does not include the mated connector interface. However, it does include potential AC-coupling capacitor attenuation on the Transmitter (TX) interconnect on a SFF-8639 module. Note that the budget allocations generally allow for a maximum of four-inch trace lengths for differential pairs having an approximate 5-mil trace width. No specific trace geometry, however, is explicitly defined in this specification. The subscripts of the symbol designators, T and R, represent the Transmitter and Receiver respectively.
3. The SFF-8639 System budget includes the mated SFF-8639 mated connector interface. See Section 5.2, for specifics on the standalone connector budget. The SFF-8639 system budget includes potential AC-coupling capacitor attenuation on the Transmitter (TX) interconnect on the system board. The subscripts of the symbol designators, T and R, represent the Transmitter and Receiver, respectively.

Note: The insertion loss budget distributions above are used to derive the eye diagram heights as described in Section 4.6. However, they are provided here only as a design guideline.

The *PCI Express Base Specification* provides design guidelines for channels designed to support 5.0 GT/s and 8.0 GT/s signaling.

B

Appendix B. Acknowledgements

The following persons were instrumental in the development of the *SFF-8639 Module Specification*: